EECS140 Midterm 1
Spring 2018

Name Key

SID

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1. [2] The LM741 op-amp looks like a single-pole amplifier with a low frequency gain magnitude of about one million and a gain magnitude of 1,000 at 1 kHz. What are the pole and unity gain frequencies?

UGB = 1000×10^3 = 1M Hz/sec A_0 = dc gain = 10^6

ω_{3dB} = 1M Hz/sec / A_0 = 1 Hz/sec

2. [6] You have made a new NMOS transistor. You measure the drain current as a function of the gate-to-source and drain-to-source voltage, and find that it is $I_d = \alpha(V_{gs}-1V)^3 V_{ds}^2$ when $1V<V_{gs}<2V$ and $1<V_{ds}<2$, where α is a positive constant with appropriate units.
   a. Write an expression for the transconductance in terms of just voltages, and in terms of I_d and some voltages.

$g_m = \frac{\partial I_D}{\partial V_{gs}} = \alpha 3(V_{gs}-1)^2 V_{ds}^2 = 3I_D/(V_{gs}-1)$

   b. Write an expression for the output resistance in terms of I_d

$r_o = 1/g_{ds}$ $g_{ds} = \partial I_D/\partial V_{ds} = 2\alpha(V_{gs}-1)^3 V_{ds} = \frac{2I_d}{V_{ds}}$

   c. Write an expression for the intrinsic gain in terms of the bias point

$A = g_m r_o = \frac{3I_D}{(V_{gs}-1)} \times \frac{V_{ds}}{2I_D} = \frac{3}{2}\frac{V_{ds}}{(V_{gs}-1)}$

   d. To maximize the gain, where would you bias this device (what voltages)?

V_{gs} = 1 V_{ds} = 2 (as large as possible)

3. [4] You have a diode with ND=10^15/cm3, NA=10^20/cm3. You calculate that the depletion width is about a micron.
   a. Is the depletion region mostly in the P side or the N side?

N-side

   b. Estimate the built-in potential at room temperature

V_{bi} = 60mV(5+10) = 0.9V

   c. If you increase the ND doping by a factor of 10,
      i. how much does the built in potential change?

V_{bi} = 60mV × 16 = 0.96 V → changes by 60mV

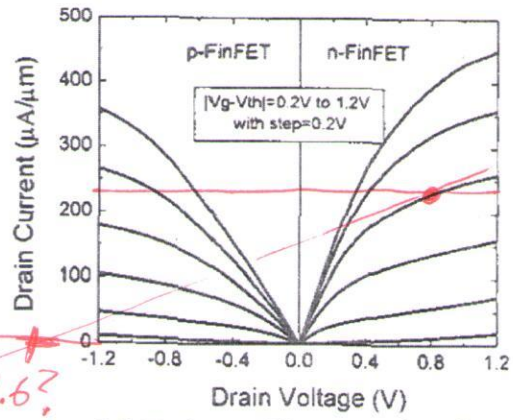
      ii. roughly how much does the depletion width change? (e.g. increase by 10x, decrease by sqrt(10), slight increase, no change, etc.)

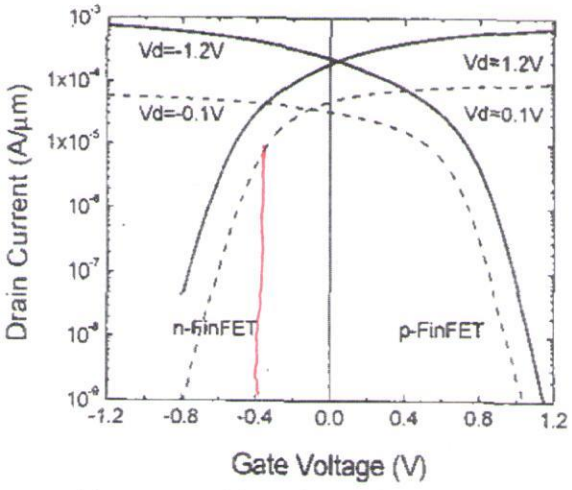
decreases by $\sqrt{10}$

4. [4] You have 10 identical diodes. You apply 1mA to one diode and measure 0.7V across it.
   a. What current do you measure if you apply 0.76V across a single diode? 10mA
   b. What voltage do you measure if you apply 1mA to 10 diodes in series? ~~0.84V~~ 7V
   c. What voltage do you measure if you apply 1mA to 10 diodes in parallel? 0.64V
   d. What voltage do you measure if you apply 2.7mA to a single diode? 0.726 or .725

$0.7 + V_{TH} =$

5. [6] The graphs below are from an AMD paper from 2002 describing preliminary results from 10nm FinFETs. You can ignore the weird threshold voltages.





$g_o \approx \frac{240\mu A}{2.4V}$

$r_o = \frac{2.4V}{0.24mA}$

10K

-1.6?

   a. [4] Estimate Id, gm, and ro for a 1um wide NMOS biased at Vds=Vgs=0.8V. What is the intrinsic gain of this device?

$I_d \approx 230\mu A$ (200-250μA OK) $\quad g_m = \frac{100\mu}{0.2V} = 0.5mA/V$

$r_o \approx 10K$ 5-20K OK $\quad g_m r_o \approx 5$

   b. [2] Estimate the NMOS subthreshold slope in mV per decade, and the parameter "n".

10^4 change in 0.4V $\quad \frac{400mV}{4 decades} \approx \frac{100mV}{decade}$

$n = \frac{100}{60} \approx 1.6$

→ or assume $V_{tn} \approx 0.2V$, $V_{gs} - V_t = 0.6V$ } $I_d \approx 150\mu A$

6. [14] You have an NMOS-input common source amplifier with a PMOS load and a large load capacitance. Both transistors are biased in saturation, and the quadratic model is appropriate. The magnitude of the gain is large (~100).

Process specs $\mu_n C_{ox}=200\mu A/V^2$, $\mu_p C_{ox}=100\mu A/V^2$, $\lambda=1/(10V)(L_{min}/L)$, $-V_{tp}=V_{tn}=1V$, $V_{DD}=5V$, $L_{min}=1um$, $C_{ox}=5fF/um^2$, $C'_{ol}=0.5$ fF/um.

You change the bias point so that you double Vov. How do the following change?

	I_D	V_{ov}	g_m	R_o	Av	ω_p	ω_u	C_{in}
double V_{ov} in quadratic	4	2	2	1/4	1/2	4	2	1/2

At a different and higher bias point, you enter into the scattering-limited velocity saturation region of operation. If you double Vov again at this operating point, what do you expect to happen

	I_D	V_{ov}	g_m	R_o	Av	ω_p	ω_u	C_{in}
Double V_{ov} in velocity saturation	2	2	1	1/2	1/2	2	1	1/2

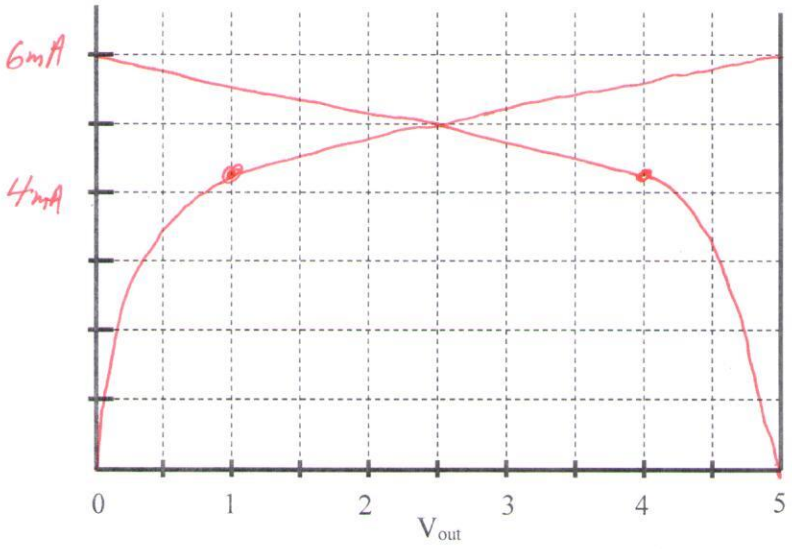
7. [9] In the same process described above, you have made a similar amplifier with $(W/L)_N=40u/1u$, $(W/L)_P=80u/1u$. You choose $V_{GSN}=2V$. Assume that the quadratic model is appropriate.
   a. [3] Carefully sketch I_{DN} vs. V_{out}. Put a dot at the transition between triode and saturation. Get the slope right in saturation.
   b. [1] What PMOS gate bias voltage will result in an output voltage of 2.5V?

V_{GP} = 3V

   c. [3] Sketch the magnitude of the PMOS current vs. V_{out} with the PMOS gate biased at V_{BP}.
   d. [2] What is the output swing?

$\{V_{out,min}\ V_{out,max}\}$ = {1, 4}

Label this axis!



label 4mA

slope correct: 6mA

V_{dsat} correct

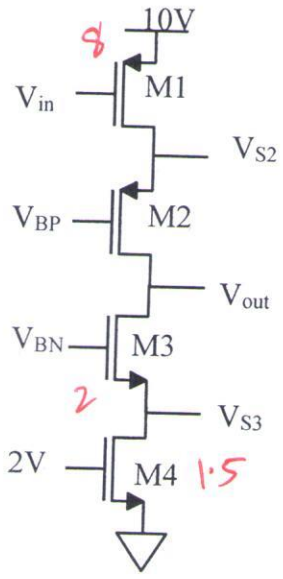
I_{do} correct

quadratic in triode
linear in saturation } 1 pt each

8. [6] Fill in the following table for a single-pole amplifier. Each row is a different amplifier.

g_m	R_o	C_L	A_{v0}	ω_p	ω_u
1m	1M	1uF	10^3	1	10^3
0.1	100	1pF	10	10G	100Grad/s

9. [11] For the circuit below, assume that $\mu_n C_{ox}(W/L)_n = \mu_p C_{ox}(W/L)_p$ and $\lambda_n=\lambda_p$ for all devices, and $V_{tn}=-V_{tp}=0.5V$. You may assume that all devices are biased in saturation, and the quadratic model is appropriate. You may assume that $\mathbf{g_m r_o >> 1}$ for all combinations (so simplify).



a. In terms of g_{m1}, r_{o2}, r_{o4}, etc., what is the impedance seen looking up from VS2?

$R_{S2up}=$ r_{O1}

b. …and looking down from VS2?

$R_{S2down}=$ $\dfrac{r_{O2}+r_{O3}+r_{O4}+g_{m3}r_{O3}r_{O4}}{(1+g_{m2}r_{O2})} \simeq g_{m2}r_{O2}$

c. What is the simplified impedance seen at VS2 and Vout, assuming that all "g_m"s are equal and all "r_o"s are equal?

$R_{S2}=$ $r_O/2$

$R_{out}=$ $g_m r_O^2/2$

d. What is the appropriate DC bias on the gate of M1?

M4 $V_{GS}=2.0V$ → I_D → $V_{DD}-2$

$V_{IN}=V_{DD}-|V_{TP}|-\sqrt{\frac{2I_D}{(W/L)_1\mu_p C_{ox}}}$ $=8.0V$

e. What is the minimum voltage for the gate of M3 such that M4 stays in saturation?

$V_{OV}=1.5V$

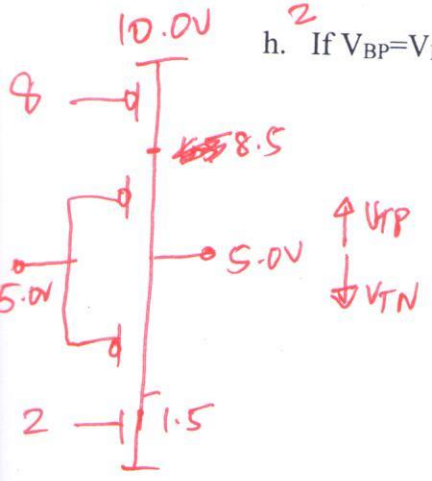
$V_{BN,min}=2V_{OV}+V_{TH,N}$ $=3.5V$

f. What is the maximum voltage for the gate of M2 such that M1 stays in saturation?

$V_{BP,max}=V_{DD}-|V_{TP}|-2V_{OV}$ $=10-0.5-3$ $=6.5V$

g. If the gates of M2 and M3 are biased according to your answers above, what is the output swing?

$\{V_{out,min}\,V_{out,max}\}=(3,7)=\{2V_{OV},\ V_{DD}-2V_{OV}\}$



h. If $V_{BP}=V_{BN}=5V$ do all devices remain in saturation? If so, what is the output swing

yes

$\{V_{out,min}\,V_{out,max}\}=\{5-V_{TN},\ 5+V_{TP}\}$

$=\{4.5, 5.5\}$