EECS140 Fall 2009 Final

Name_____

SID_____

Prob.	Score
1	/35
2	/40
3	/20
4	/30
5	/20
6	/30
7	/25
Total	/200

1) Give a short answer for each of the following questions. One sentence is usually enough.
   a) One of your friends in 140 this semester was trying to run their bandgap amplifier off of the regulated analog voltage supply. Why didn't their system work?

   b) Your SPICE simulations for an amplifier in feedback show that you have a gain error of less than 0.4%. When you get the real chips back, you discover that lambda, λ , for all of your devices is actually several tens of percent smaller than what you simulated. Your bias currents did not change. Will your closed-loop gain error change? Explain how and why, or why not.

   c) For the same situation as the previous problem, will your closed-loop pole frequency and unity gain frequency change? Explain how and why, or why not.

   d) For the ADC in your project, the handout showed the positive input of the op-amp hooked to ground. Most of you didn't end up doing that. What did you hook it to, and why?

e) For the PGA in your project, the handout showed that the positive input of the op-amp was hooked to ground. For those who implemented the circuit that way, why did it cause a problem for the op-amp design, and what was the solution?

f) For the analog voltage regulator in your project, many groups saw 10MHz noise on both the bandgap voltage and the regulated analog output. What was a likely cause of that problem?

g) For the digital voltage regulator in your project, many groups saw V_{DDD} oscillations at frequencies different from 10MHz. What was a likely cause of that problem?

2) In some non-standard process you have a two-stage CMOS op-amp with the following specs (similar in some ways to your project's digital regulator):

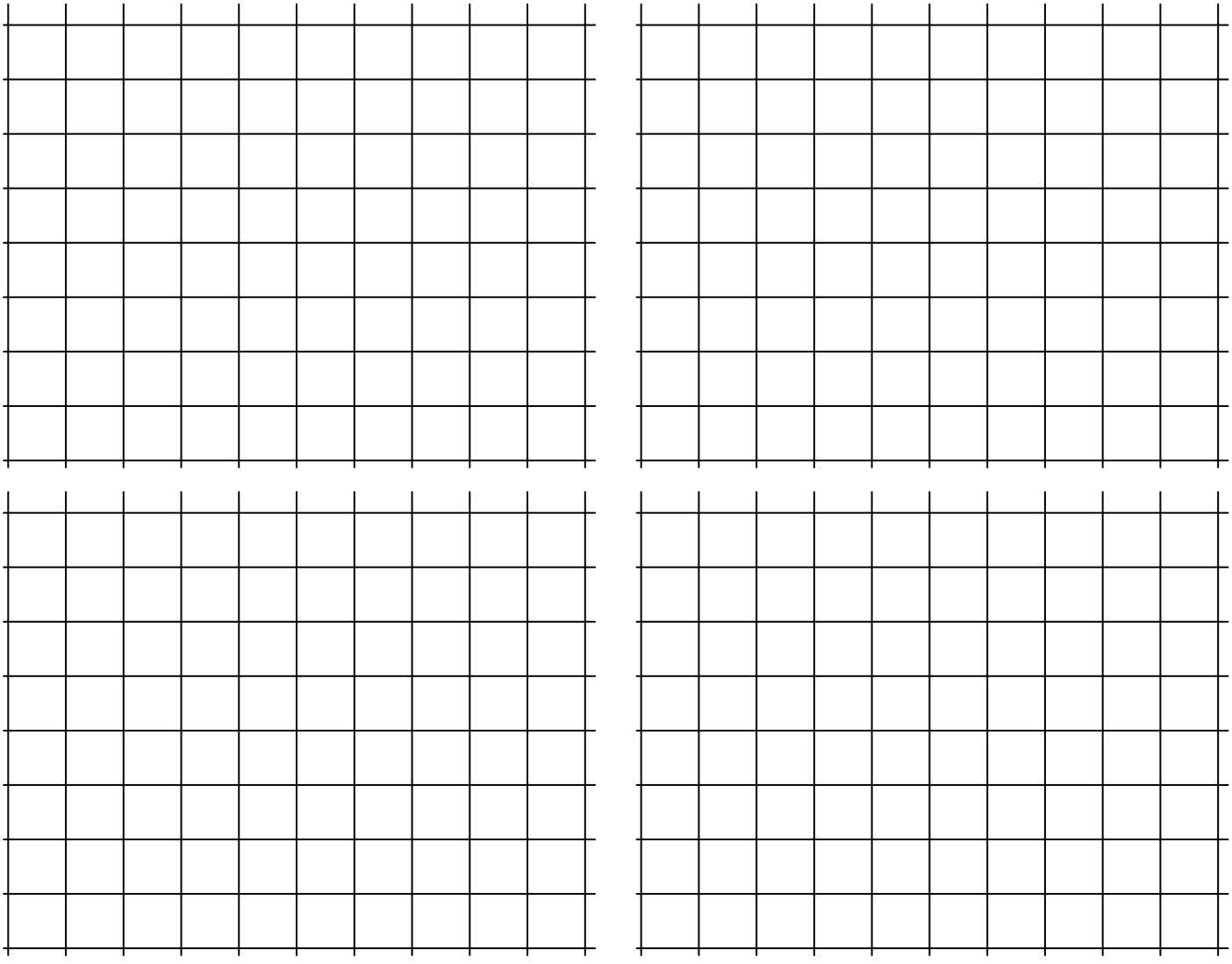
- R_{o1}= 100k, G_{m1}=1ms, C_1=10p
- R_{o2} = 100 Ohms, G_{m2}=1 S, C_2=1nF

You want to use the amplifier in unity gain feedback.

A) If the compensation capacitor C_C is zero, what is the frequency of the first and second poles? What is the unity gain frequency? What is the phase margin?

ω_{p1}	
ω_{p2}	
ω_u	
PM	

The grids below are provided merely for your convenience. You don't need to plot anything for this problem (but it might help you get the right answers!).



B) If you were to add 1pF to C_C, what is the change in the two pole frequencies, and the unity gain frequency that would result? (I want an answer in radians/sec) In this case, what is the feedback factor f for which this amplifier has 45 degrees of phase margin?

ω_{p1}	
ω_{p2}	
ω_u	
f	

C) Starting from the original C_C=0 case again, if you want to get 45 degrees of phase margin in unity gain feedback, you can add capacitance to one of three nodes. How much capacitance would you need to add to C_1 to get 45 degrees of phase margin? What if you only added capacitance to C_2? What if you only added capacitance to C_c, with a series resistor R_Z? What value should you use for R_Z?

Add to C_1	
Add to C_2	
Add to C_c	
R_Z	

3) You need to design an op-amp to run off of a single-sided 2.5V supply. The positive input will be at 1V and the output must swing from 0.6 to 1.4V. The amplifier will be used in feedback with a closed-loop gain of 5, driving a 100fF load. The gain error needs to be less than 2% at 1Mrad/sec.

a) Based on this information, which of the following topologies might work to implement the opamp? (circle the letters of those that might work)
   a) NMOS input folded cascode
   b) PMOS input folded cascode
   c) NMOS input 2 stage Miller compensated
   d) PMOS input 2 stage Miller compensated
   e) NMOS input telescopic cascode
   f) PMOS input telescopic cascode

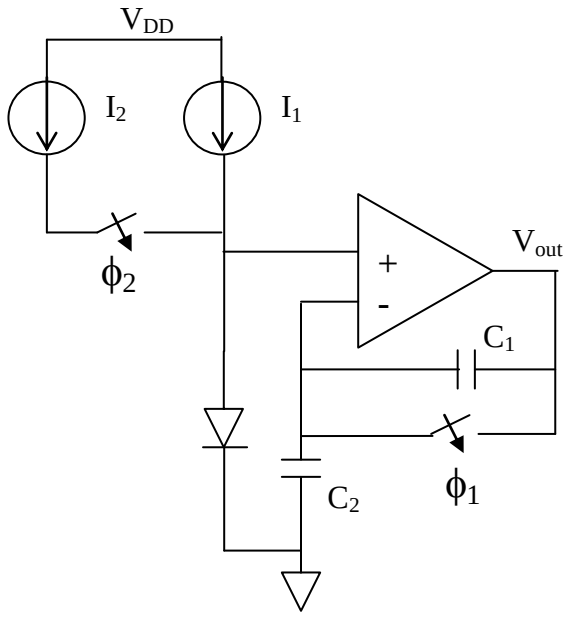
   For those that would NOT work, explain why:

b) What is the minimum unity gain frequency of your op-amp, ω_u?

c) What is the minimum current that must be burned in each of the input differential pair transistors?

4) You need to design a bandgap reference in a process with very poor quality resistors. You've found a circuit topology (below) that might work and you need to analyze it. Assume ϕ_1 and ϕ_2 are non-overlapping clocks and $I_2 = 2\ I_1$. You may assume that the op-amp is ideal. The diode has a saturation current I_S.

a) What is the current and voltage on the diode during ϕ_1?



b) during ϕ_2?

c) What is the approximate temperature coefficient of the diode voltage in either phase?

d) What is the voltage difference between the voltage on the diode during ϕ_1 and ϕ_2? What is special about this voltage? What is it's temperature coefficient?

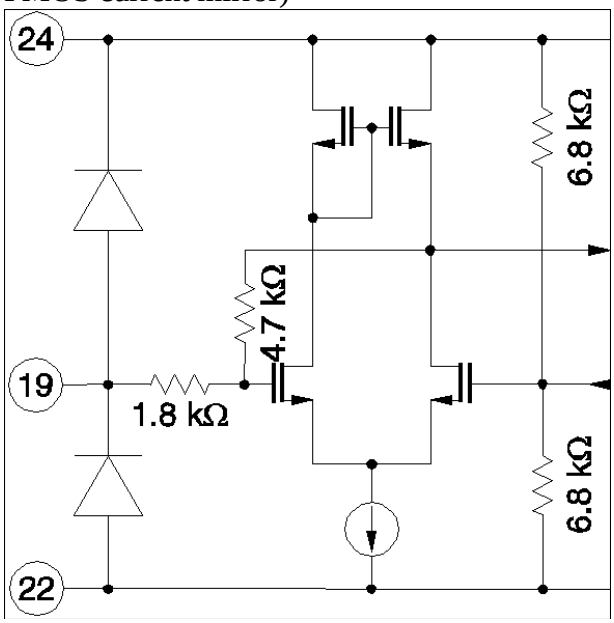
e) What is V_{out} during ϕ_1?

f) What is the change in V_{out} from ϕ_1 to ϕ_2?

g) Write an expression for V_{out} during ϕ_2.

h) How would you pick the values of the capacitors to make V_{out} supply and temperature independent?

5) The figure below comes from the datasheet for the NEC UPB1009K GPS receiver. The figure shows one of the analog inputs to that chip. Pins 22 and 24 are GND and V_{DDA} respectively, and pin 19 is an off-chip input. (Note: the current mirror is actually PMOS – they just drew it wrong in the datasheet. Answer this question assuming a PMOS current mirror)

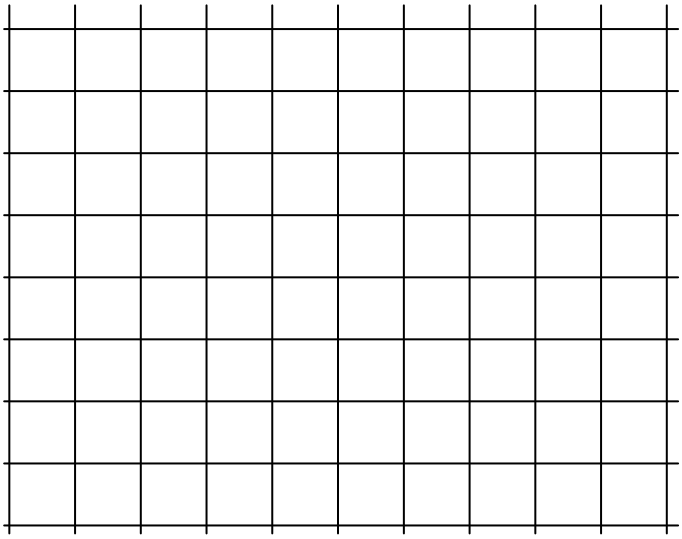


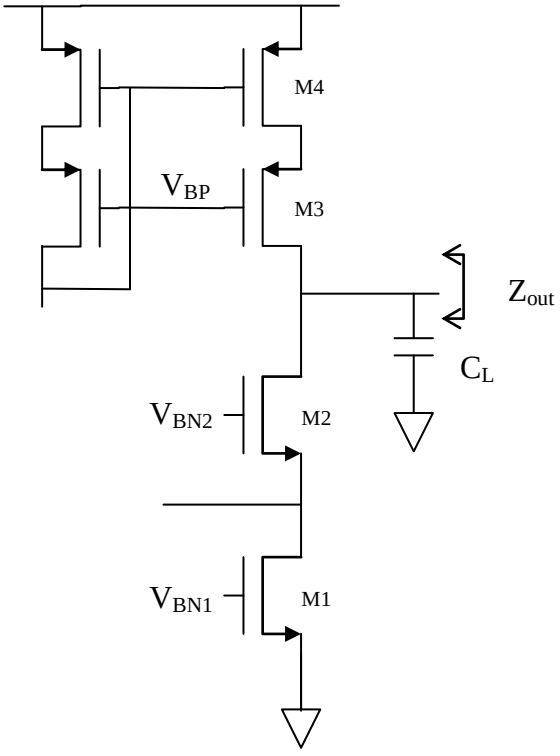
a) Assuming that the diodes are ideal, what impact do they have on the circuit?

b) What is the topology? (draw the transistors as an op-amp) You can ignore the diodes now.

c) Is the feedback positive or negative? What do you think that this circuit does?

6) We talk about a folded cascode being a "single-stage" amplifier and having a single dominant pole. In a PMOS-input folded cascode, there is a pole associated with the source of the NMOS cascode transistor M2. Your job is to explain why this pole is above the unity gain frequency. Naïvely, one might think that the cascode pole is at the frequency where the impedance of C_{GS2} becomes smaller than the DC impedance seen looking into the source of M2. Assuming that g_m=1ms and r_o=100k for all transistors, C_{GS2}=100fF, and C_L=1pF,
Calculate the "naïve" (incorrect) pole location described above.
Plot the output impedance of the amplifier, Z_{out}.
Plot the impedance seen looking into the source of M2.
Calculate the pole frequency associated with this node.





7) The graph on the following page is taken from the EIMAC 4-65A vacuum tube datasheet (1962). The solid lines are curves of constant plate current, as a function of grid voltage and plate voltage. You can ignore the screen and grid current. With a plate current of .100 Amps and a plate voltage of 2500V, estimate g_m, r_o, and the gain of this amplifier.

g_m	
r_o	
A_V	