EECS140
HW4, due Thursday 9/24 at 8am
(This was Midterm 1, Spring 2008)

Name_____

SID_____

Prob.	Score
1	/10
2	/30
3	/20
4	/15
5	/25
Total	

1) Fill in the following table. Do NOT use a calculator!

dB	Power ratio
13	
-7	
16	
-1	
-9	
1	
17	
4	
-14	

2) Design an NMOS-input common source amplifier with a PMOS load with a low frequency gain of approximately 200, a unity gain frequency of 1G rad/sec with a 1pF load, and an output swing of at least 500mV to 2V with a 2.5V single-sided supply. Clearly indicate what values you are using for g_m, r_o, I_D, V_{dsat}, gate bias, W, L for each transistor. Assume our standard process model.

	g_m	r_o	I_D	V_{dsat}	V_G	W	L
NMOS							
PMOS							

3) Fill in the following table where each row is a different single-pole amplifier

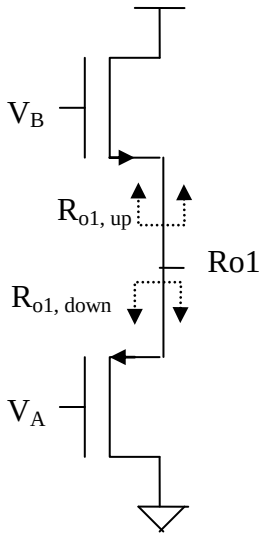
G_m [S]	R_o [Ω]	C_L [F]	Av	ω_p [rad/s]	ω_u [rad/s]
50u	1M	50f			
		100f	200	40M	
30m			150		15G
	1M			50M	25G

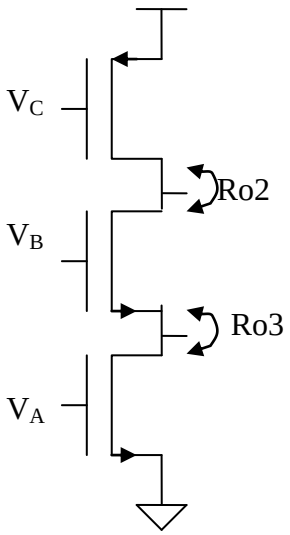
4) You have a single-pole amplifier with a gain of 20 at 200MHz, and a low frequency gain of 1000. What is the gain at 100kHz, 10MHz, and 2GHz?

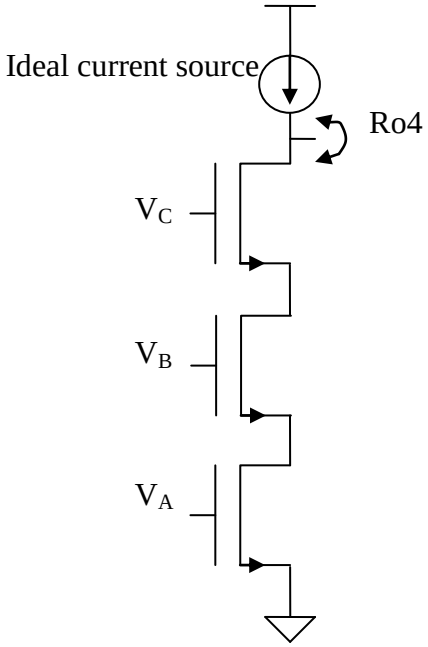
Frequency	Gain
100kHz	
10MHz	
2GHz	

5) What is the total low frequency impedance and the low frequency impedance seen "looking up" and "looking down" at the output node indicated in each circuit? Write your answer in terms of g_{mp} , $g_{mn,}$ r_{on}, and r_{op}. Assume that all nmos devices have transconductance g_{mn} and output resistance r_{on}, and all pmos devices have transconductance g_{mp} and output resistance r_{op}. Write the full expression for up and down, and then the simplified total impedance assuming that gm*ro >> 1 for all combinations of gm and ro. You may ignore all capacitors.

	Full expression	Simplified expression for Ro, assuming gm ro >>1
$R_{o1,\ up}$		
$R_{o1,\ down}$		
$R_{o2,up}$		
$R_{o2,down}$		
$R_{o3,up}$		
$R_{o3,down}$		
$R_{o4,up}$		
$R_{o4,down}$		







Additional hw4 questions (not from the previous midterm):

6) What is the low frequency input capacitance seen at nodes A, B, and C in the previous problem?
7) What is the input capacitance at those nodes at frequencies above the unity gain frequency for the amplifier?
8) For the amplifier you analyzed in HW3, problem 4, (CS PMOS input 100/1 for both devices w/ NMOS gate bias of 0.8V), estimate the input capacitance seen at low frequency, and above unity gain.
9) Plot the magnitude and phase of the impedance seen looking into the input of your HW3 problem 4 amplifier. Make sure that your plots make sense at low and high frequency, based on your estimates above.

Useful things to think about, but not due as homework:

- what is the gain from any node to any other node in the circuits in problem 5?
- what is the input impedance vs. frequency for any node in the circuits in problem 5?