EECS140 Midterm 2
Spring 2008

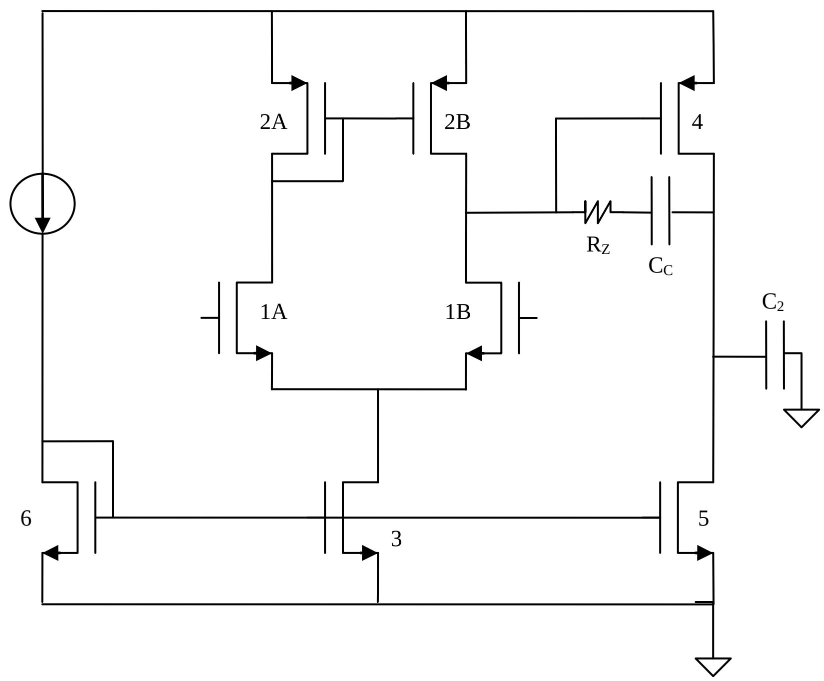
Name____________________________

SID_____________________________

Prob.	Score
1ABCDIJ	/20
1EFGH	/30
2	/15
3	/15
4	/20
Total	

1) For questions 1A and B, give your answers in terms of the various g_m, C_{gs}, V_{dsat}, $V_{TH,}$ (e.g. g_{m1}, C_{gs5}), and C_C, C_2
Unless otherwise indicated, you may make the following assumptions:

- All transistors are biased in saturation
- All capacitors are assumed to be zero except C_C, C_2 , and C_{gs} for all transistors.
- $g_m r_o >> 1$ for all combinations of g_m and r_o



1A) What is the minimum supply voltage that can be used which will keep all devices in saturation?
1B) Due to a layout error, one version of this amplifier has $(W/L)_{2B}$= 5 $(W/L)_{2A}$. Derive the mirror pole frequency, and the corresponding mirror/diff-pair zero frequency.

1A) $V_{DD,min}$	
1B) ω_{PM}, ω_Z with layout error	

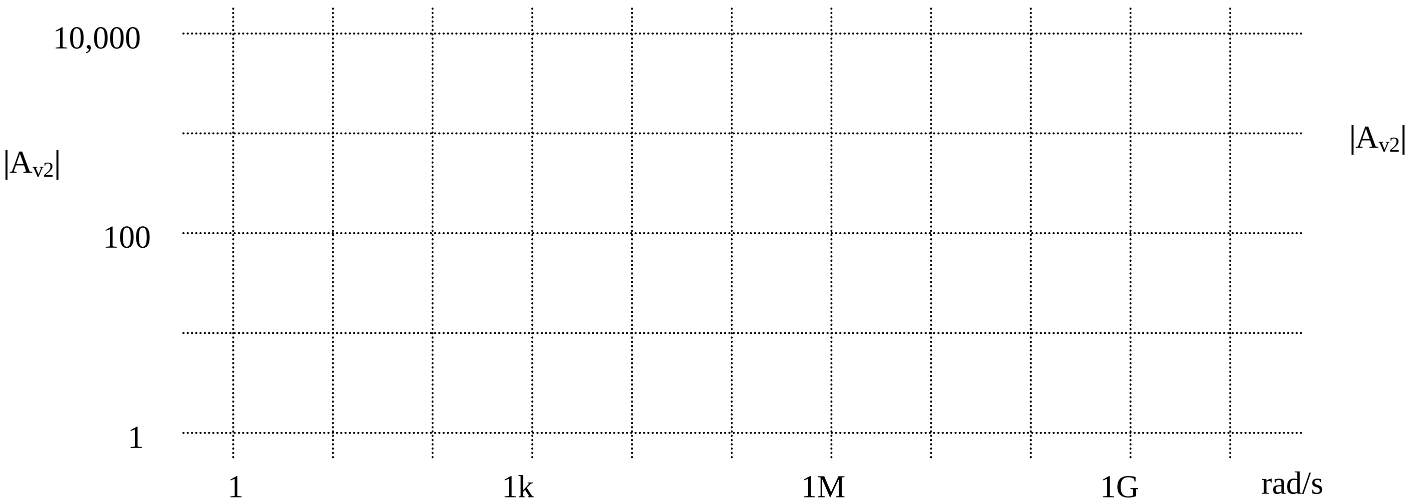
Prob. 1, cont.) Assume that the layout error in 1B is fixed, and the mirror doublet is at high frequency and can be ignored. Using the following values for parameters, answer the following questions

$g_{m1,2}$	$r_{o1,2}$	g_{m4}	$r_{o4,5}$	C_2	C_C	C_{gs4}
0.1mS	2M	10mS	200k	100p	1p	10p

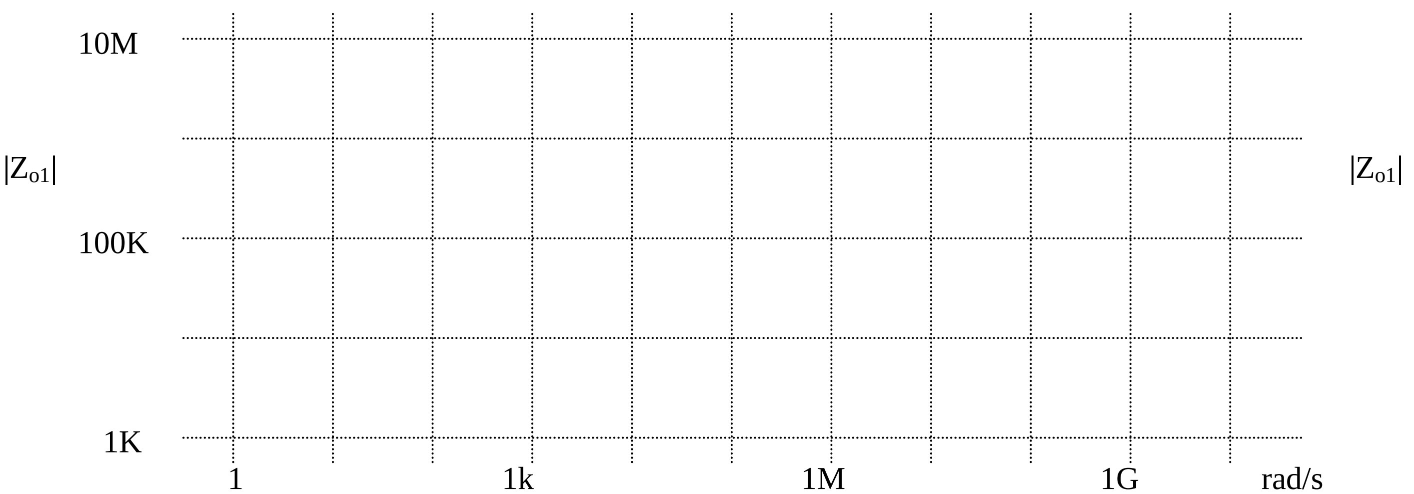
1C) Why is R_Z in the circuit, and what value should it have?
1D) What are the uncompensated poles (C_C=0) ?
On the following pages,
1E) plot the magnitude of the second stage gain
1F) plot the overall impedance seen at the first stage output (including R_{o1}, C_{gs4}, C_C, and any effects of Miller multiplication),
1G) plot the magnitude of the first stage gain,
1H) plot the magnitude and phase of the overall gain. **Label any poles and zeros clearly**.
1I) Estimate the phase margin for this value of C_C.
1J) Approximately what value of C_C is needed for a 45 degree phase margin?

1C) R_Z purpose and value	
1D) $\omega_{p1,0}$, $\omega_{p2,0}$	
1I) Phase margin, C_C=1p	
1J) C_C for 45 degree phase margin	

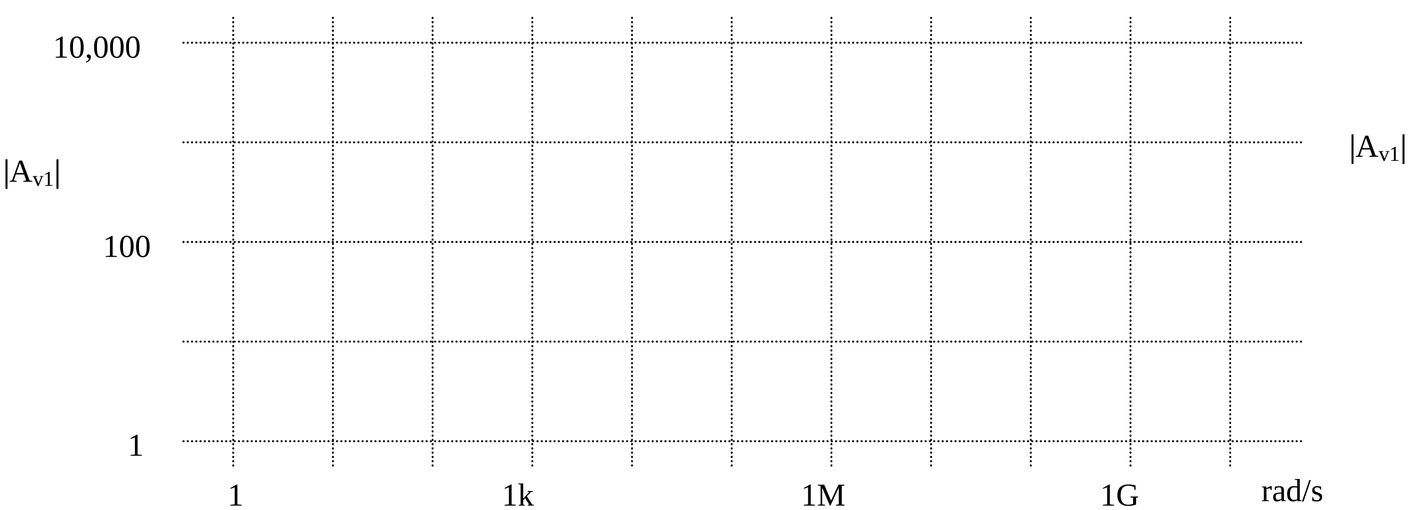
1E) Second stage gain – $|A_{v2,0}|$



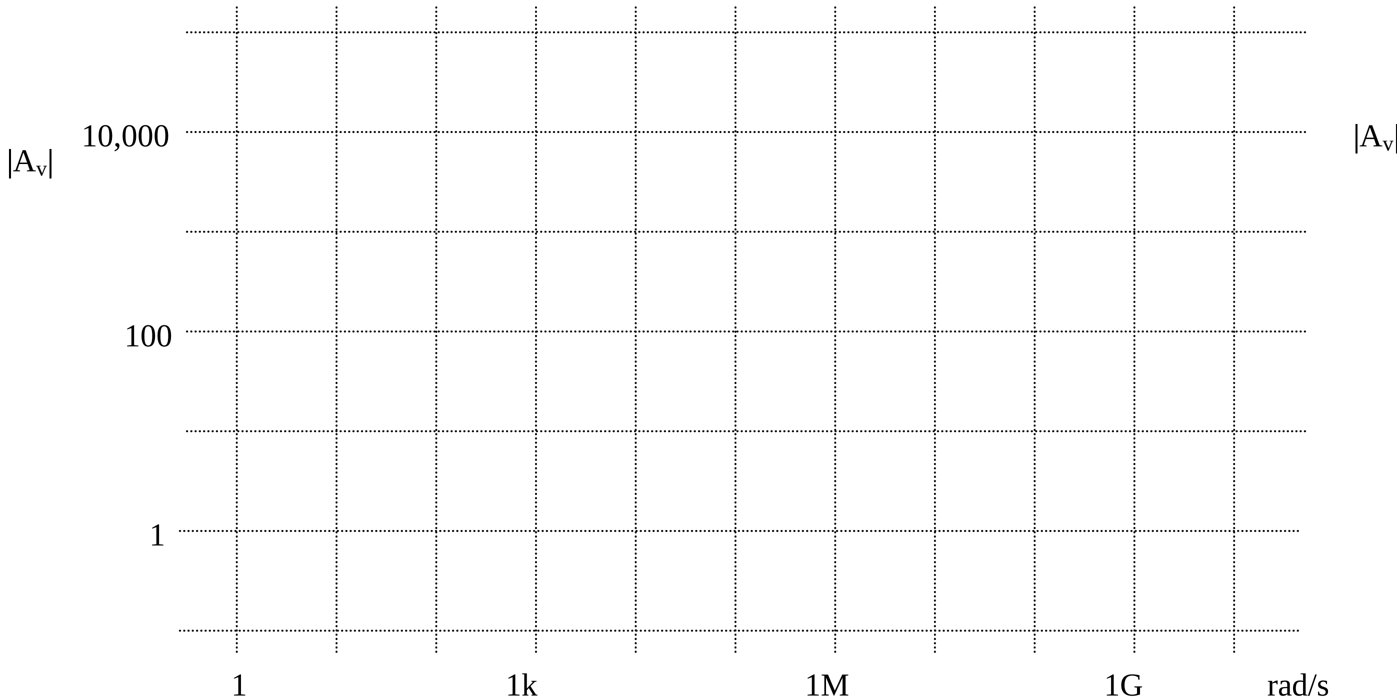
1F) Impedance at first stage output, $|Z_{o1}|$



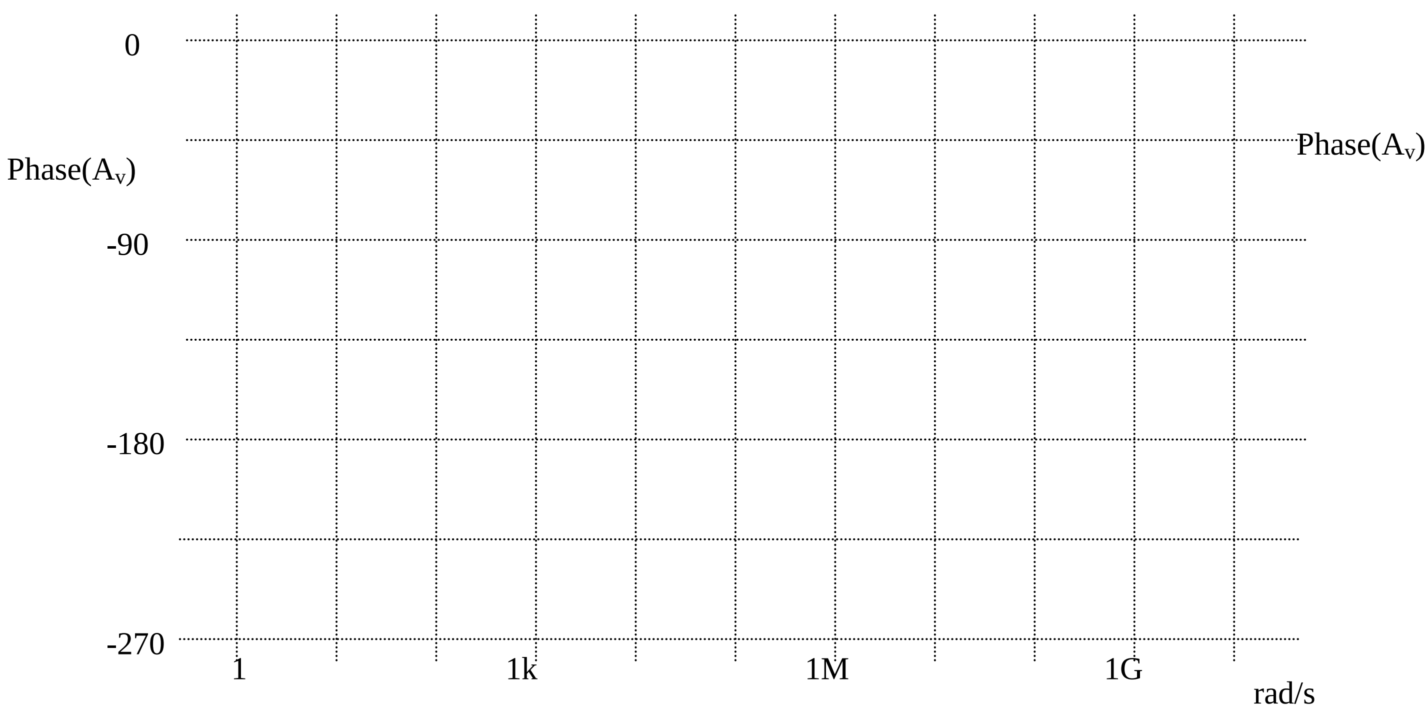
1G) First stage gain, $|A_{v1}|$



1H) op amp Bode plot



Label any poles and zeros clearly!



2) For the following questions, give a short answer and justification (2 sentences max).
2A) For lab1, how did the input common mode value affect the current in the first stage? (a lot, a little, not at all)

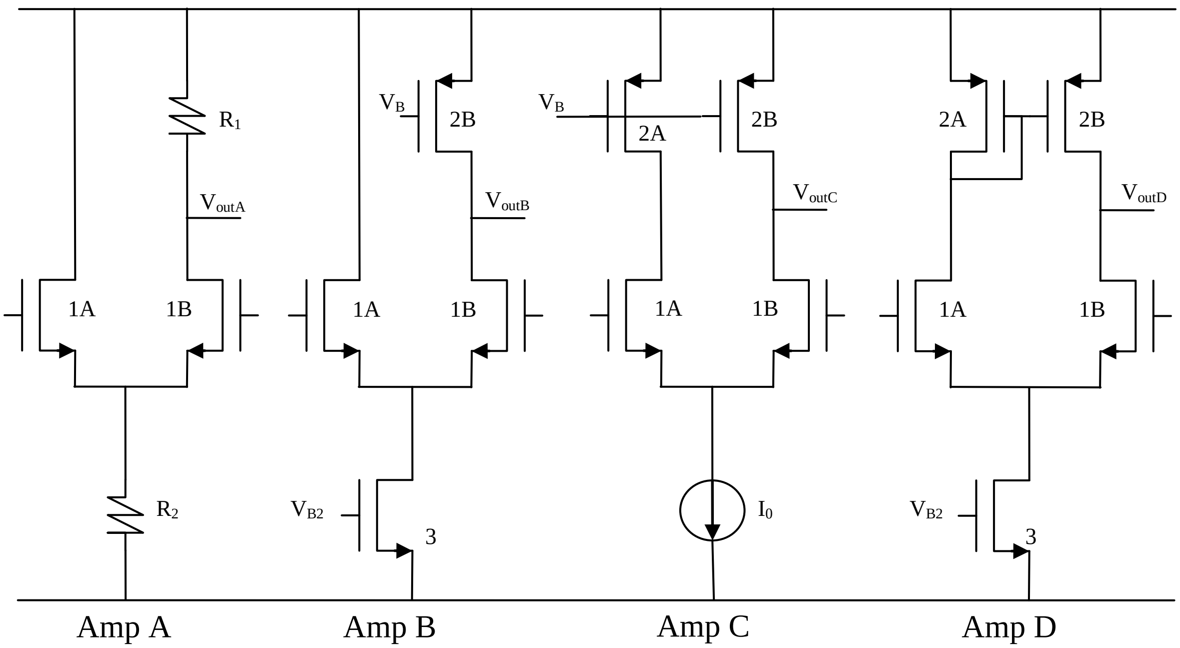
2B) For lab1, how did the input common mode value affect the gain of the first stage? (a lot, a little, not at all)

2C) For lab1, does that circuit work with resistive feedback? Why or why not?

3) for your Miller-compensated 2-stage amplifier in problem 1 with a phase margin of 45 degrees, what is the impact on the compensated pole locations of doubling C_1? Doubling C_2? Doubling C_c? (answers might be double, half, minimal effect, …)

	ω_{p1}	ω_{p2}
Double C_1		
Double C_2		
Double C_c		

4) For the four differential amplifiers below, assume that $1/g_m << R << r_o$ for all configurations, and that current sources are ideal. Calculate the common mode and differential gain for each amplifier.



	A_{VCM}	A_{VDM}
Amp A		
Amp B		
Amp C		
Amp D		