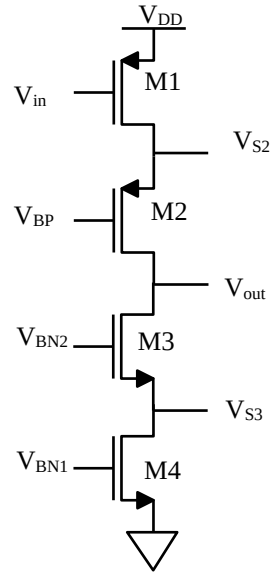
E 140/240A Prof. Pister
Spring 2018

Homework Assignment #4

Due by online submission **Wednesday** 2/14/2018 (Thursday 9am)

1. 16spMidterm1C problem 6
2. Look at Midterm 1, Fall 09, problem 1. For each device, swap NMOS/PMOS, but keep the same region of operation, magnitude of overdrive if appropriate, and magnitude of drain/source voltage.
3. Using the process parameters from the previous homework, design an NMOS-input common source amplifier with a PMOS load with a low frequency gain of approximately 200, a unity gain frequency of 1G rad/sec with a 1pF load, and an output swing of at least 300mV to 2.2V with a 2.5V single-sided supply. Minimize power consumption. Clearly indicate what values you are using for gm, ro, ID, Vdsat, gate bias, W, L for each transistor. Clearly indicate which parameters you "pick", and which you solve for. Calculate the input capacitance.
4. How much could you change the input capacitance above if you were primarily optimizing that?
5. An NMOS common source amplifier has a 10V supply and a 1kΩ load (to the supply) in parallel with 100pF. Assume $\mu_n C_{ox}$=20uA/V^2, W/L=10,000/1, V_{tn}=1V, λ=0.01V. You should be able to do all of the calculations by hand (without calculators). One-ish significant digits is fine.
   a. Write an expression for I_D as a function of output bias point. How much does I_D change as the output voltage varies from 9V to 1V?
   b. What is the change in the input and overdrive voltage as the output varies from 9V to 1V?
   c. Write an expression for g_m and r_o as a function of output bias point.
   d. Write an expression for A_{v0} as a function of output bias point.
   e. For each of the output bias points {9V, 6V, 1V}, calculate the current in the device, g_m, r_o, A_{v0}, ω_p, and ω_u . Fill in a table with those columns.
6. For the circuit below, assume that $\mu_n C_{ox}(W/L)_n = \mu_p C_{ox}(W/L)_p$ and $\lambda_n=\lambda_p$ for all devices. You may assume that all devices are biased in saturation, and the quadratic model is appropriate. You may assume that $g_m r_o$ >>1 for all combinations.



   a. Why must all devices have the same overdrive voltage?
   b. What is the DC bias on the gates of M1 and M4?
   c. What is the minimum voltage for the gate of M3 such that M4 stays in saturation?
   d. What is the maximum voltage for the gate of M2 such that M1 stays in saturation?
   e. If the gates of M2 and M3 are biased according to your answers above, what is the output swing (minimum to maximum voltage for both M2 and M3 to remain in saturation)?
   f. What is the impedance seen "looking up" and "looking down" at the output, and the total impedance?
   g. What is the impedance looking up and down at the source of M3, and the total impedance?
   h. Is the total impedance seen at the source of M2 different from the source of M3? Why or why not?
   i. What is the gain from the input to the output?
   j. What is the gain from the input to the source of M2?
   k. What is the input capacitance?
   l. With a total output capacitance of C_o, what are the pole and unity gain frequencies?
7. In the circuit above, if you double the overdrive voltages on all devices, how does that affect the swing, DC gain, pole frequency, and unity gain frequency?
8. [ee240a] How do your answers change if you want to make this a nanopower (sub-Vt) amplifier, or the fastest possible (velocity saturated) amplifier? If you made this amplifier with Intel 14nm finfets, what ranges of gain, swing, and bandwidth could you get?