E 140/240A Prof. Pister
Spring 2018

Homework Assignment #3

Due by online submission **Tuesday** 2/6/2018 (Wednesday 9am)

1. A single-pole amplifier has a low frequency gain of 1000, and a gain of 2 at 500MHz. What are the pole frequency and unity gain frequency in Hz? What is the gain at 10MHz?
2. The parameters for a particular 0.5um CMOS process are C_{ox}=5fF/um^2, C'_{ol}=0.5fF/um, $\mu_n C_{ox}$=200μA/V^2, $\mu_p C_{ox}$=100μA/V^2, λ=1/(10V) for L=0.5um, $-V_{tp}=V_{tn}$=0.5V, V_{DD}=2V. You are designing an NMOS-input common source amplifier with a PMOS load. The input capacitance of the next stage is 100fF. Assume that sub-threshold and inversion currents are equal when the overdrive voltage is 10mV.
   a. If $(W/L)_n$=10/0.5 and $(W/L)_p$=20/0.5 and V_{IN}=0.7V
      i. Using the quadratic model, carefully plot I_{dn} vs. V_{out} from 0 to VDD. Label the axes. Draw a dot to clearly separate the triode region from the saturation region. Is the quadratic model a good fit for this device and bias condition? Explain why or why not.
      ii. Choose the PMOS gate bias such that the output bias point is at mid-rail (1V in this case). What are V_{ovn} and V_{ovp}? Are they different? Why or why not?
      iii. Plot $|I_{dp}|$ vs. V_{out} on the same plot as you used for the NMOS. Estimate the output voltage swing (the output voltage range over which both devices remain in saturation).
      iv. Calculate G_m, R_o, ω_p, and ω_u (assuming the input capacitance of the next stage dominates the output pole).
      v. Calculate C_{gs}, C_{gd}, and C_{in} for this amplifier
      vi. If the amplifier were driven by another copy of itself, calculate the input pole frequency
   b. For the same amplifier, if V_{IN}=0.5V, and the PMOS gate bias is set so that the output bias is at mid-rail
      i. What model should be used for the transistors?
      ii. What drain current will flow?
      iii. Calculate G_m, R_o, ω_p, and ω_u
      iv. Calculate C_{gs}, C_{gd}, and C_{in}
      v. If the amplifier were driven by another copy of itself, calculate the input pole frequency
   c. For the same amplifier, if V_{IN}=1.5V, output biased mid-rail
      i. What model should be used for the transistors?
      ii. Choose the PMOS gate bias such that the output bias point is at mid-rail
      iii. What drain current will flow?
      iv. Calculate G_m, R_o, ω_p, and ω_u
      v. Calculate C_{gs}, C_{gd}, and C_{in}
      vi. If the amplifier were driven by another copy of itself, calculate the input pole frequency
   d. Comment on the bandwidth and power consumption of these three operating points
3. Write down a table of settling error vs. time for t/τ={1,3,5,7}. Use a calculator for this one. Memorize the table to one significant digit.
4. An RC low pass filter with a time constant of 1μs is driven with a 0--1V square wave. Sketch the first full cycle of the input and output when the square wave is first turned on, and
   a. If the frequency of the square wave is 1kHz
   b. If the frequency of the square wave is 1MHz
   c. If the frequency of the square wave is 1GHz
5. A common source FET amplifier has a resistive load and λ=1/(50V). If the output is biased at 5V, the transistor is in saturation, and the resistive load has the same impedance as the output resistance of the transistor. What is the supply voltage?
6. Fill in the following table

A_{v0}	ω_p	ω_u		g_m	r_o	C_L
1000	1M					1p

	1M	0.1G			100k	
		10G			1M	20f
	10	10M				10p

7. For a quadratic model MOSFET, sketch the following curves. No axis labels needed, but try to get the shape right, and label with something like "goes as sqrt(X)" or "linear in X"
   a. g_m vs. V_{GS} with W/L constant
   b. g_m vs. V_{GS} with I_d constant
   c. g_m vs. I_d with W/L constant
   d. g_m vs. I_d with V_{GS} constant
   e. g_m vs W/L with I_d constant
   f. g_m vs W/L with V_{GS} constant
8. [ee240A] Same as problem 6, but for sub-Vt, and weak/moderate inversion (good luck)