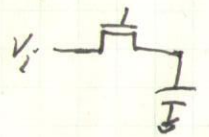
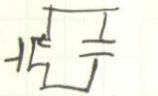
switches
MUX
ADC (DAC)

Last time

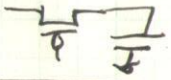
$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L} V_{OV}} \quad \text{(} V_{OV} = V_{DD} - V_{tn} \text{)}$$



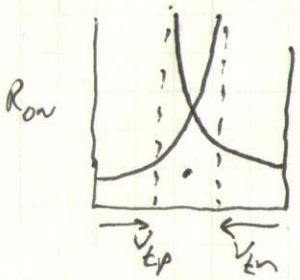
$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{tn} - V_i)}$$

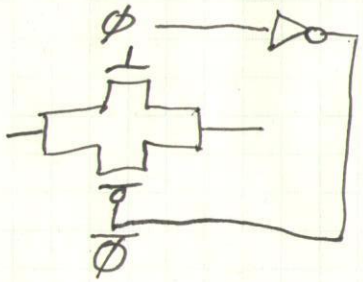


$$R_{ON} = \frac{1}{\mu_p C_{ox} \frac{W}{L} V_{OV}}$$



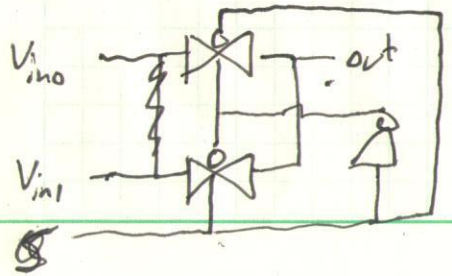
$$R_{ON} = \frac{1}{\mu_p C_{ox} \frac{W}{L}(V_i - V_{tp})}$$

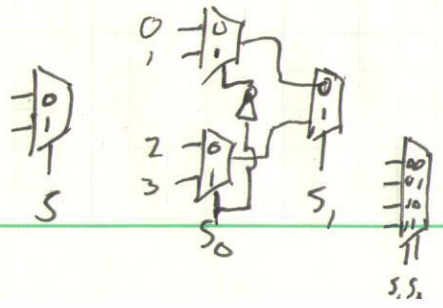


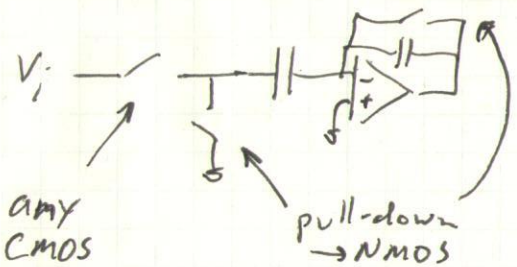


butterfly gate
CMOS switch

analog MUX

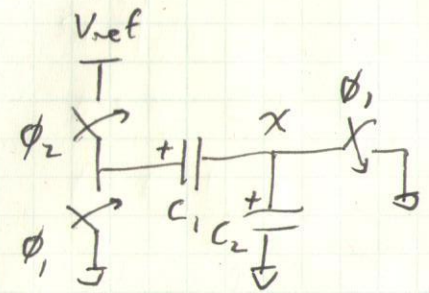


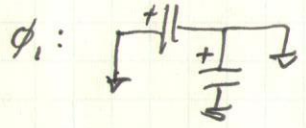




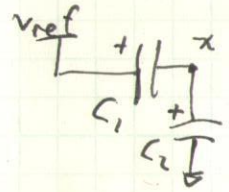
FETs which ~~switch~~ for which switch?

ADC → CAP DAC





$Q_1 = Q_2 = 0 \quad Q_x = 0$

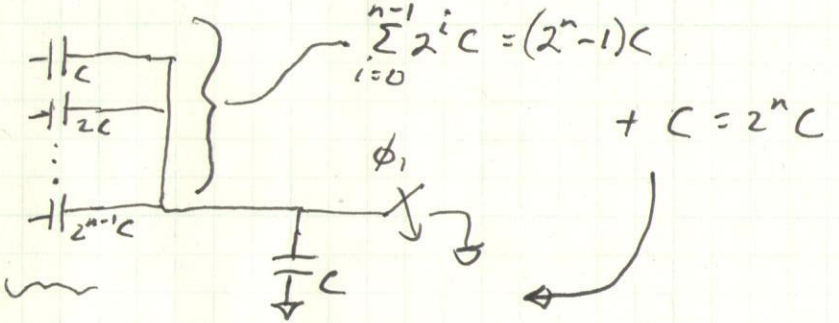


$$Q_x = Q_{1-} + Q_{2-} = 0$$

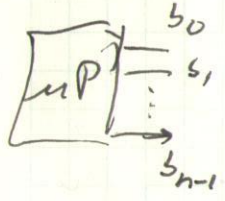
$$= -C_1(V_{ref} - V_x) + C_2 V_x = 0$$

$$C_1 V_{ref} = (C_1 + C_2) V_x \qquad V_x = \frac{C_1}{C_1 + C_2} V_{ref}$$

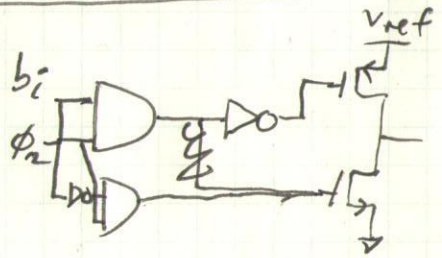
make a binary weighted array for C_1: C, 2C, 4C, 8C, ...
control w/ µP
$C_2 = C + \{$whatever is not in $C_1\}$



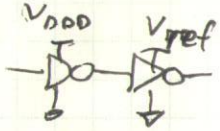
Q: How do you select what goes in C_1 and C_2?
A: Where the left side is switched on ϕ_2.



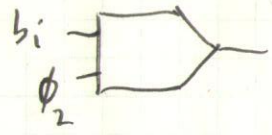
V_{DDD} domain



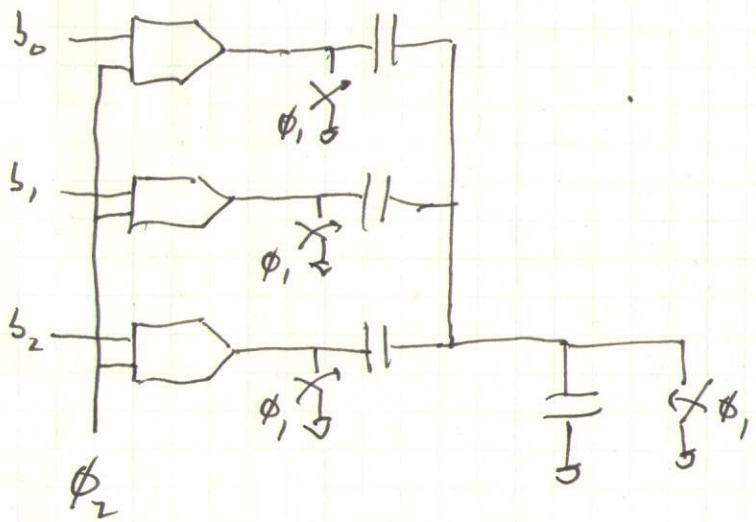
V_{ref} ~~V_{DDA}~~ domain



beware of signals crossing power domains (and clock domains)



ϕ_2	b_i	
0	X	Z
1	0	0
1	1	1



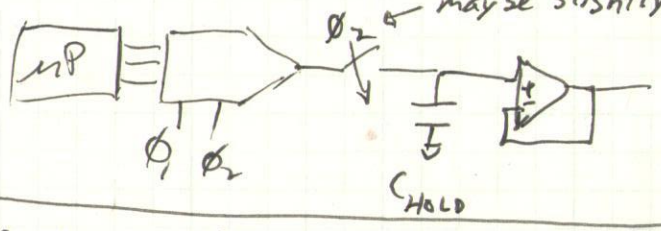
$C_1 = BC \qquad C_2 = (2^n - B)C$

$B = [b_2, b_1, b_0]$

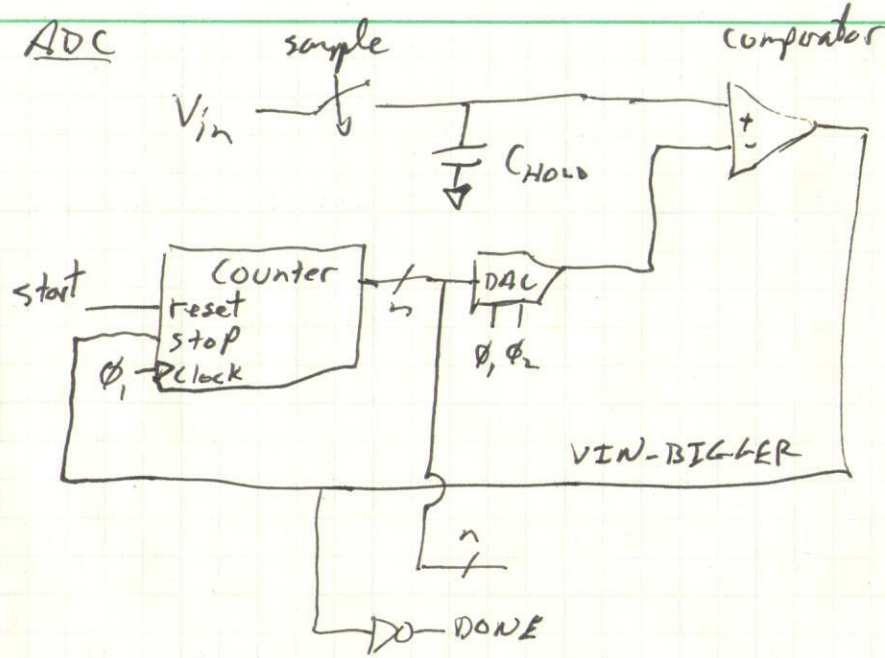
slow

$b_2 b_1 b_0$	C_1	C_2	V_0
0 0 0	0C	8C	0
0 0 1			$\frac{1}{8} V_{ref}$
0 1 0			$\frac{2}{8} V_{ref}$
⋮			
1 1 1	7C	C	$\frac{7}{8} V_{ref}$

$$V_0 = \frac{C_1}{C_1+C_2} V_{ref} = \frac{BC}{BC+(2^n-B)C} V_{ref} = \frac{B}{2^n} V_{ref}$$



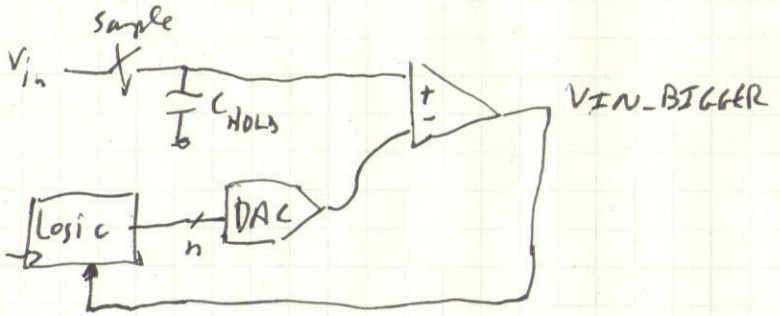
ADC



Problems: slow

variable conversion time

SO Successive Approximation



set $s_i := 0 \ \forall i = 0..n-1$

~~set~~ for $i = n-1, i \geq 0, i--$

{

set b_i

if (VIN_BIGGER == 0) reset s_i;

}