Project

presn this week (12)
division of labor, intro
presn week 14
design review

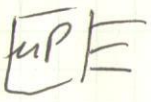
in class RRR week

HW9

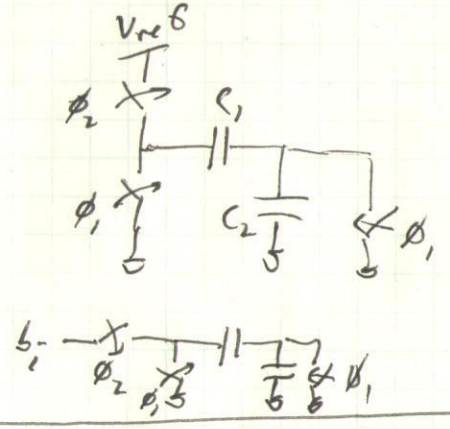
SC ADC

switched cap DAC, ADC

last time

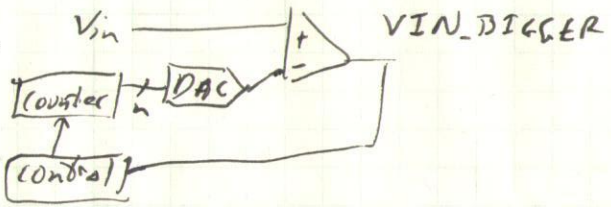


b_i

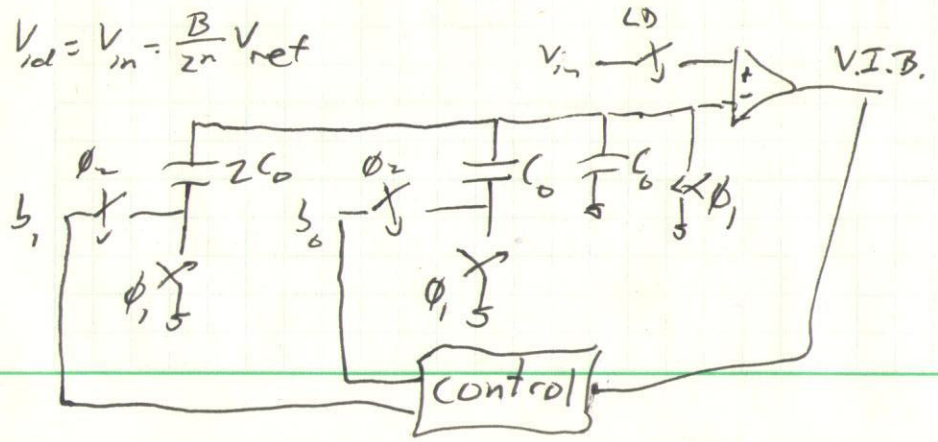


now we have a DAC

simplest ADC



$V_{id} = V_{in} - \frac{B}{2^n} V_{ref}$

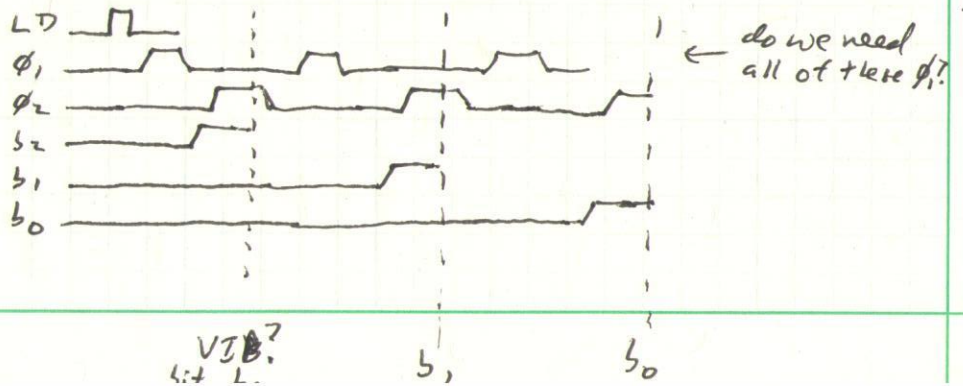


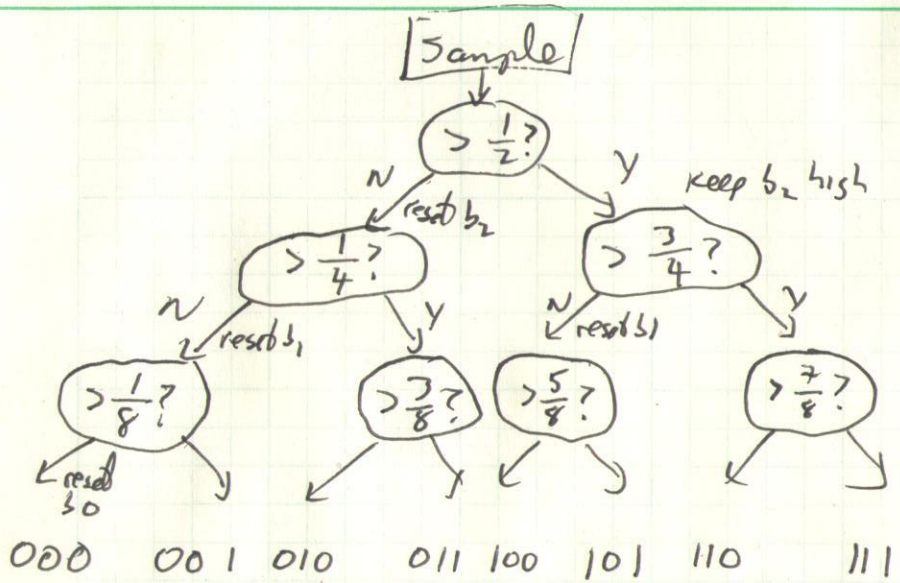
binary search is better than linear

3 bits $b_2 b_1 b_0$ 4 caps: $4C_0, 2C_0, C_0, C_0$

$V_- = \frac{B}{8} V_{ref}$ during ϕ_2

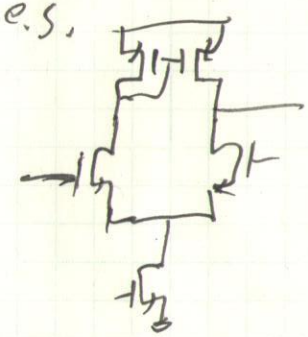
$V_{id} = V_{in} - \frac{B}{8} V_{ref}$ during ϕ_2



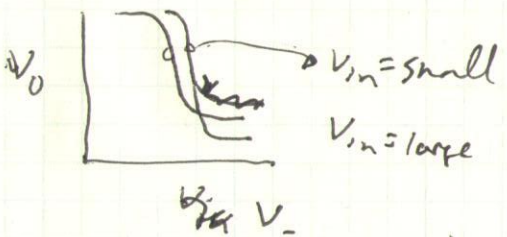


problem: tough to set comparator offset $< 1/2$LSB over $(0, V_{DD})$

e.g.

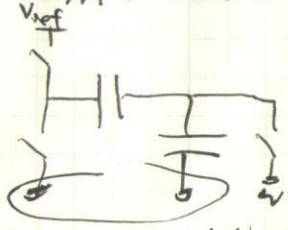


i) V_{cm} varies $(0, V_{DD})$ — hard!



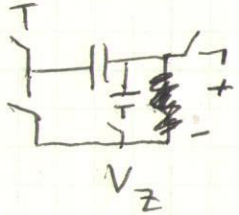
V_{icm} changes the decision point $\Leftrightarrow$ input offset

need to find a way to compare at same voltage no matter V_{in}. How? SC cleverness

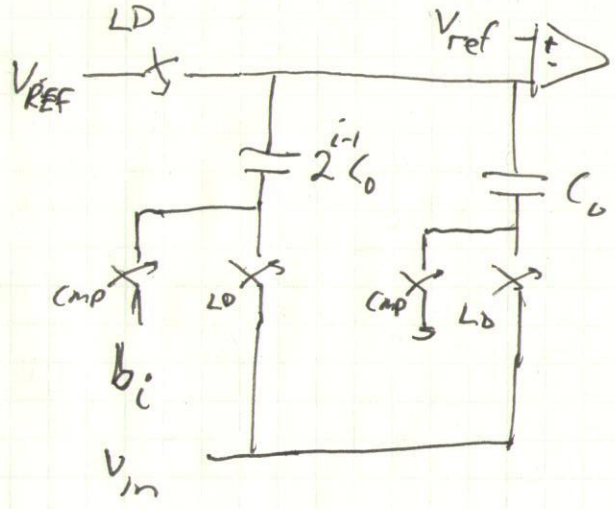
Recall  $V_x = \frac{B}{2^n} V_{ref}$

Lab: if this is set V_z?

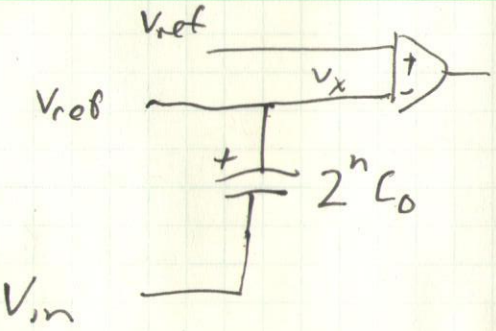
initial voltage on caps is V_z then change redistb.

 $V_x = \frac{B}{2^n} V_{ref} + V_z$

make $V_z = V_{ref} - V_{in}$ then $V_x = \frac{B}{2^n} V_{ref} - V_{in} + V_{ref}$



During the LD phase



$Q_{x,LD} = (V_{ref} - V_{in}) 2^n C_0$

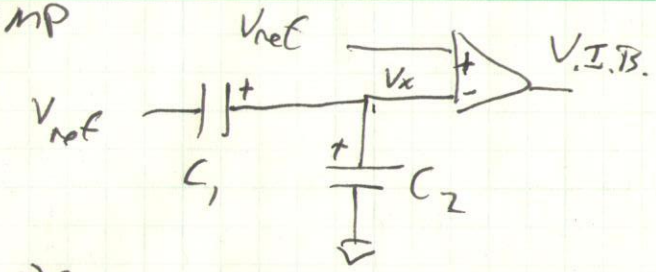
this charge is fixed when LD goes low

How long will it stay?

100ks/s, 10μV in 1 sigma

assume 1pf cap, 1pA leakage ⇒ 1V/s

During CMP



$C_1 = BC_0$

$C_2 = (2^n - B) C_0$

$Q_{x,cmp} = (V_x - V_{ref}) C_1 + V_x C_2$

$= (C_1 + C_2) V_x - V_{ref} C_1$

which we know $= Q_{x,LD} = (V_{ref} - V_{in}) 2^n C_0$

$$(V_{ref} - V_{in}) 2^n C_0 = V_x (2^n C_0) - V_{ref} B C_0$$

$$V_{ref} - V_{in} = V_x - V_{ref} \frac{B C_0}{2^n C_0}$$

$$V_x = V_{ref} + V_{ref} \frac{B}{2^n} - V_{in}$$

$$V_{id} = V_{ref} - V_x = V_{in} - V_{ref} \frac{B}{2^n}$$

one problem: if V_{in} small, during 1st compare

$b_n = 1$ $V_x \approx 1.5 V_{ref}$

Can be an issue