Debussing
Project
presenters results
test harness

regulators

Integration
ideal models done ASAP
VCVS op-amps, comparator
start integrating

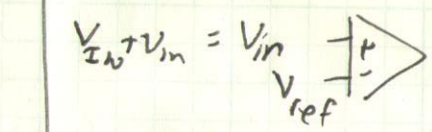
Debussing

DC voltages
DC currents
g_m, r_o values
run DC sweeps
} compare to hand calcs

Don't hack!

be careful of high gain amplifiers

$V_{IN} + V_{in} = V_{in}$

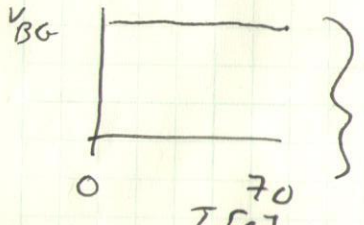


if $A_v = 10{,}000$ what is the width of the useful input voltage range?

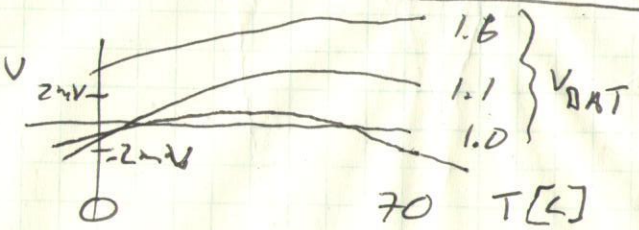
presenting results

Bandgap works
ADC doesn't work
} both useless

$V_{BG} = 1.25V$ - under what conditions?



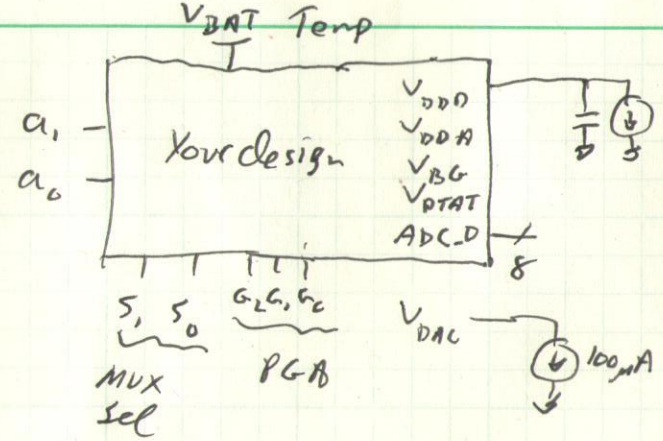
} better, but how much error?
V_{DD} variation?



plot so that you show the error over temp, over V_{DD} incl. outside the needed range until it breaks

140/140A 18SP W12L2

test harness



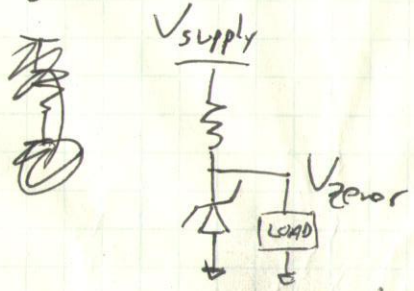
Regulator

most circuits like to run at a fixed voltage

battery varies a lot

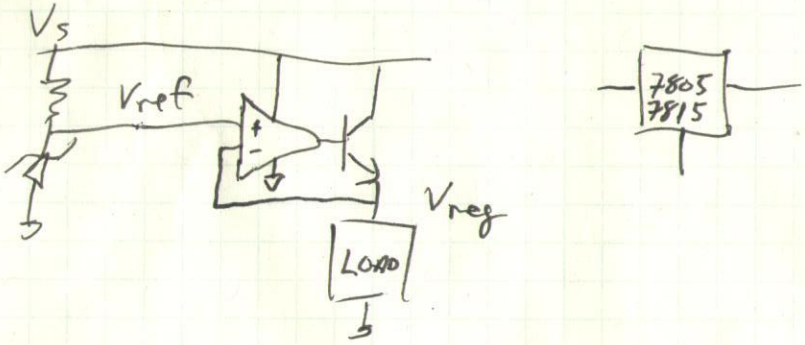
⇒ use a voltage regulator

old days:



horribly inefficient!
varies a lot

Today: reference voltage + op-amp + transistor



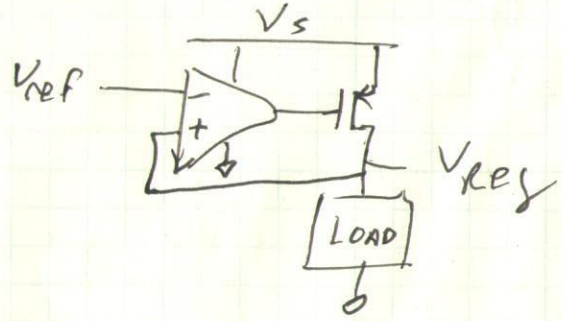
Best case, need $V_S \geq V_{reg} + V_{DS}$

(probably worse w/ op-amp swing)

$\geq 0.6V$ overhead or "drop out"

~~Low regulator~~

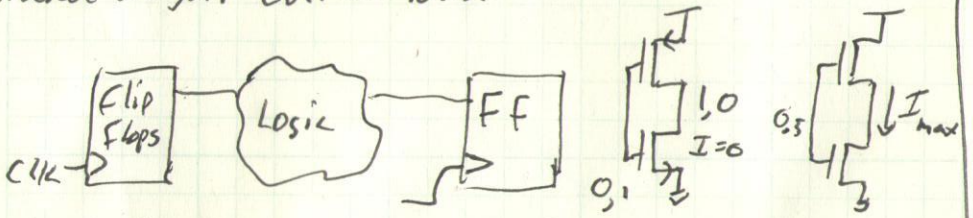
Low Drop Out regulator (LDO)



Need $V_S \geq V_{reg} + V_{ov,p}$

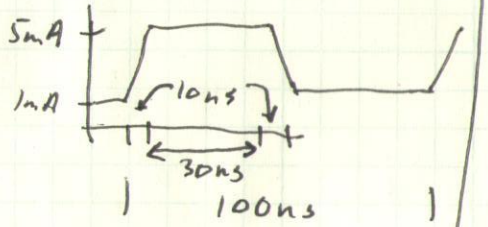
↳ ~100mV drop-out or less

model of µP current load



lots of gates switch on rising edge of CLK

leakage, plus lots of spikes



excess charge per cycle:

$Q = (4mA)(40ns)$

$= 160pC = 0.16nC$

$\overline{I} = 1mA + \frac{0.16nC}{100ns} = 2.6mA$

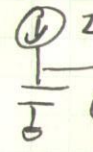
$\frac{2.6mA}{10MHz} = 260\frac{\mu A}{MHz}$ probably a little high for 40nm process, but maybe.

10 MHz probably low

(100K gates)(10 fF/gate) = 1nF capacitance.

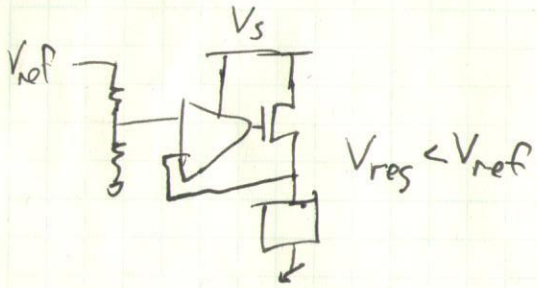
↑ mostly wiring

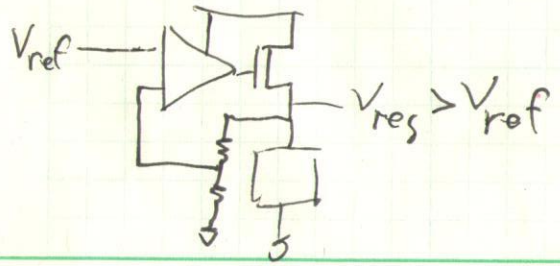
with constant current



$\Delta V_{pulse} = \frac{\Delta Q}{C} = \frac{0.16nC}{1nF} = 160mV$

V_{reg} different from V_{ref}





Stability

2 extremes

1) op-amp very slow

PMOS gate tracks average current

2) op-amp fast, dominant pole at output

output ~ const

PMOS gate moving a lot at 10 MHz