Project

FINAL DESIGN due < 2 weeks (9 AM Monday 4/30)
all cadence files to enable testing

Final Presentation in RRR week: upload before presn.
sign up

2^{nd} presn to me next week: sign up

Wafer sort - acceptance testing
binning based on performance
trim w/ OTP
BIST - memories

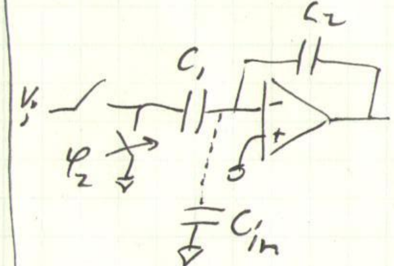
1¢/s?

≈ die cost?

LTC1968 - 4 opamps, comparator, switches ⇒ ≈ $10 digikey in 1,000s

PGA issues

Gain = 8, $f = ?$ $1/8$? no.

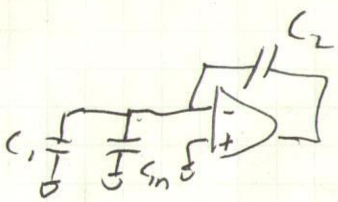


$\left.\frac{V_o}{V_i}\right|_{\text{end of } \varphi_2} = \frac{C_1}{C_2}$

C_{in} is parasitic capacitance on node V_-

$\approx C_{gs1}$

during φ_2



$$f = \frac{C_2}{C_1 + C_2 + C_{in}}$$

even if $C_{in} = 0$ $f \neq \frac{1}{gain}$

e.g. $G = 8 = \frac{C_1}{C_2}$ $f = \frac{C_2}{8C_2 + C_2} = \frac{1}{9}$

if $C_{in} \approx C_2 \Rightarrow f = \frac{1}{10}$

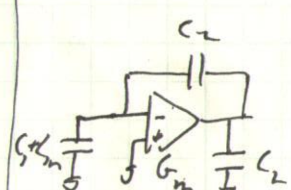
small effect on both time constant and precision

$$\frac{V_{out}}{V_{in}} = \frac{C_1}{C_2} \frac{1}{1 + \frac{1}{Af}} \approx \frac{C_1}{C_2}\left(1 - \frac{1}{Af}\right) \quad \text{eqn 13.53}$$

↑ error term

time constant

$$\tau = \frac{1}{fG_m}\left(C_2 + f(C_1 + C_{in})\right) \quad \text{eqn 13.59}$$



⇒

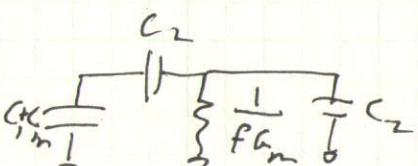
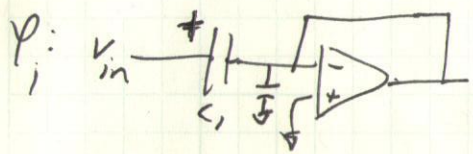


fig 13.52

High freq: $i_o = G_m V_-$, $V_- = fV_o$ $\Big\}$ $\frac{V_o}{i_o} = \frac{1}{fG_m}$

What about C_{in} and our Q calc?



$$Q_- = -C_1 V_{in} \rightarrow V_- C_{in}$$

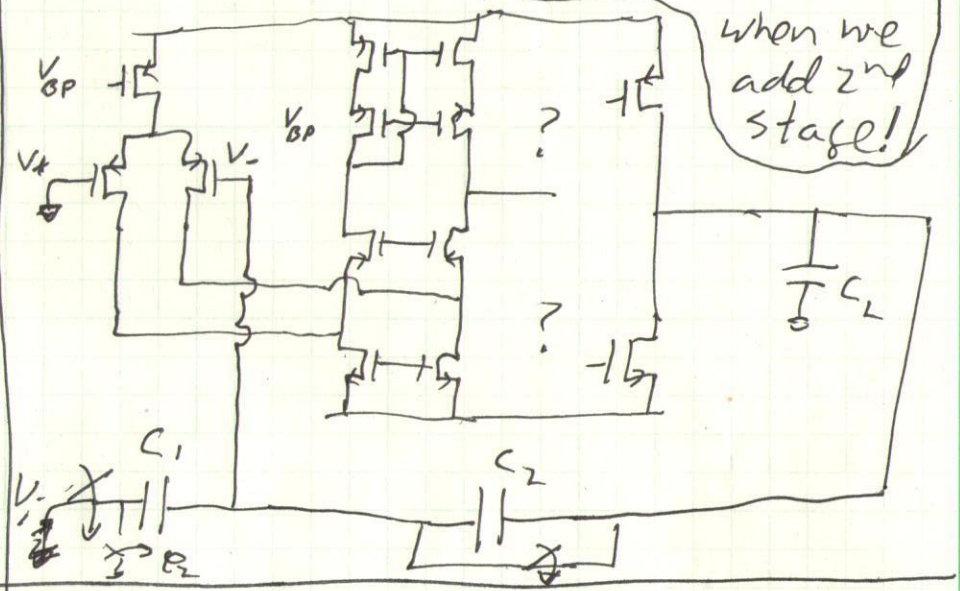
↑ ideally 0

really: input offset, finite gain

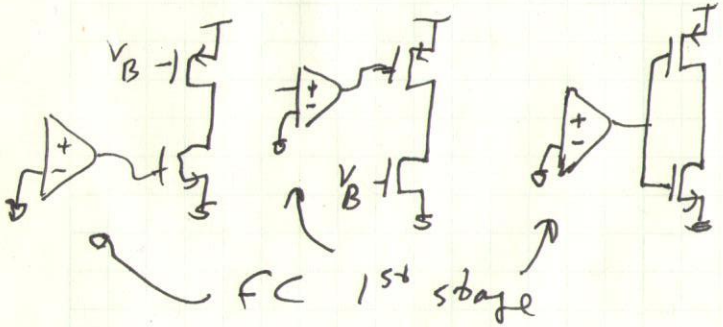
some error on Q_-

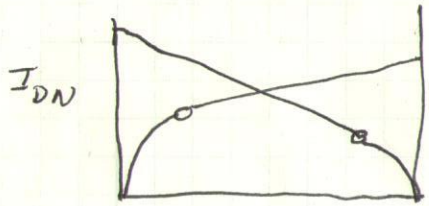
Pulling to ground

SWAP V_+, V_- when we add 2nd stage!



Connect 1st stage output to NMOS, or PMOS? or both?

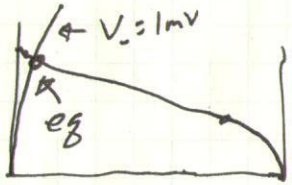




Need to drive V_{out} to 0 w/ capacitive load.

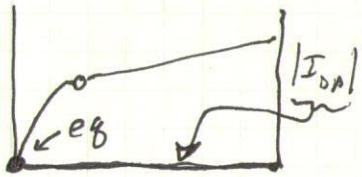
↳ ≈ 0, $< V_{LSB}$

If FC has a gain of 1,000, then V_{out} = 1mV will rail the output of the FC 1st stage.



Connect NMOS

Big increase in NMOS current, but probably doesn't pull V_o low enough



Connect PMOS

Need to get 1st stage output > $V_{DD} - |V_{tp}|$

CMOS may work too, but big cross-over currents possible