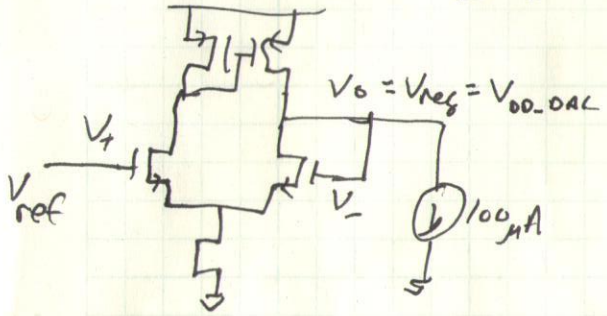
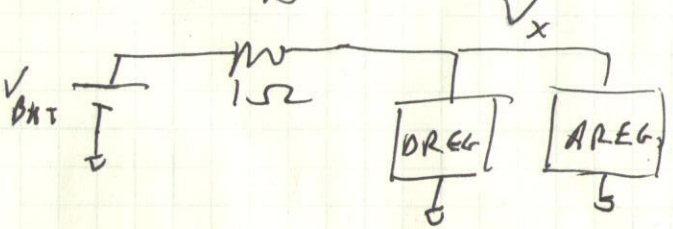
Regulators DREG: ✓ dominant pole at V_{reg}.

DAC_REG: Don't know capacitance

100 μA current - do we need a 2nd stage?



~~Charge injection~~



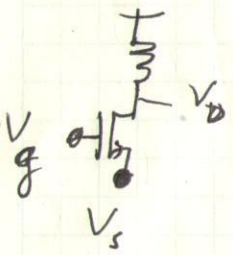
If DREG tracks I_{DDD} perfectly (V_{DDD} has no ripple)

then how much ripple on V_x?

$\Delta V_x = (1\Omega)(4mA) = 4mV$

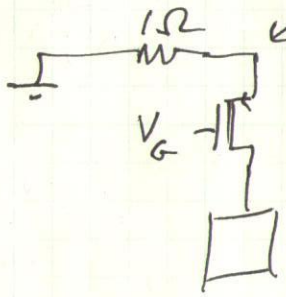
problem? maybe

Consider



$A_{G\to D} = -g_m R_D$

$A_{S\to D} = +g_m R_D$



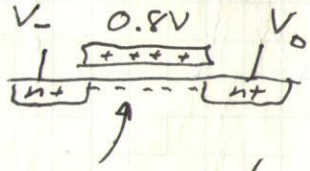
← 4mV ripple @ 10MHz

if V_G is constant, could be a big ripple on V_{REG}

Can be trouble for bandgap as well

Power Supply Rejection Ratio

Charge injection



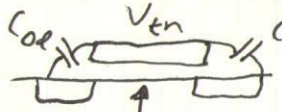
$Q_{channel} = (V_{DD} - V_{tn}) C_{ox}$

Fast falling edge of clock: assume charge splits

$\frac{1}{2} Q_c$ ← → $\frac{1}{2} Q_c$

slow clock

$Q = C_{ol} V_{tn}$

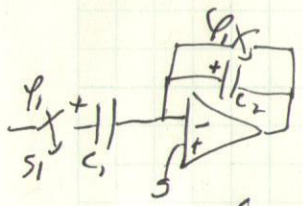


≈ no charge when $V_{gs} = V_{tn}$

switch is now off

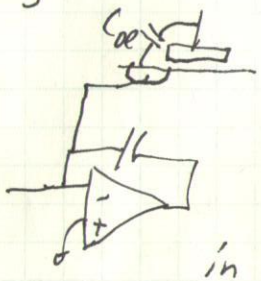
1/10/2014 1:55 PM 4/13/13

say $C'_{oe} = 1 fF/\mu m$ $\quad W = 1\mu m \Rightarrow C_{oe} = 1fF$



recall $Q_- = -V_{in} C_1 + \cancel{V_-}(C_{in} + C_2)$

but now $+ V_{DDA} C_{oe}$



slow clock ⇒

when $V_G = V_{tn}$

$$Q_- = -V_{in} C_1 + V_{tn} C_{oe}$$

in ϕ_2 $\quad V_o = \frac{-Q_-}{C_2} = \frac{C_1}{C_2} V_{in} - \frac{C_{oe}}{C_2} V_{tn}$

say $C_2 = 4ff$ $\quad V_{tn} = 0.3V$

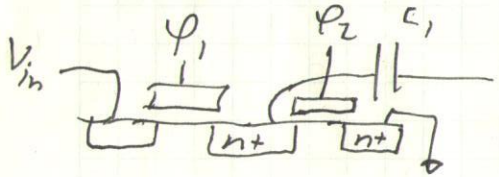
$$V_o = \frac{C_1}{C_2} V_{in} - \underbrace{\frac{1ff}{4ff}(0.3V)}_{75mV \text{ error}}$$

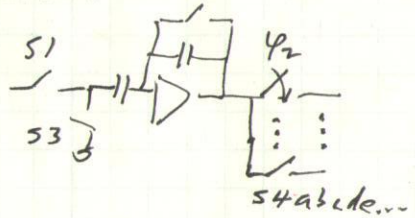
so make switches as small as possible ← W

use big enough C_2

note that both of these make discharge of C_2, V_- slower - there are limits

what about the other switches?





charge injection of ϕ_2 irrelevant on PGA

but on ADC? want S3 after S4

on S1, only a problem if it ~~does~~ turns off

before S2

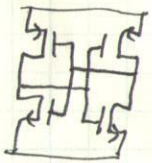
Strong ARM

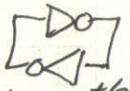
for comparator, can use op-amp + inverter

or

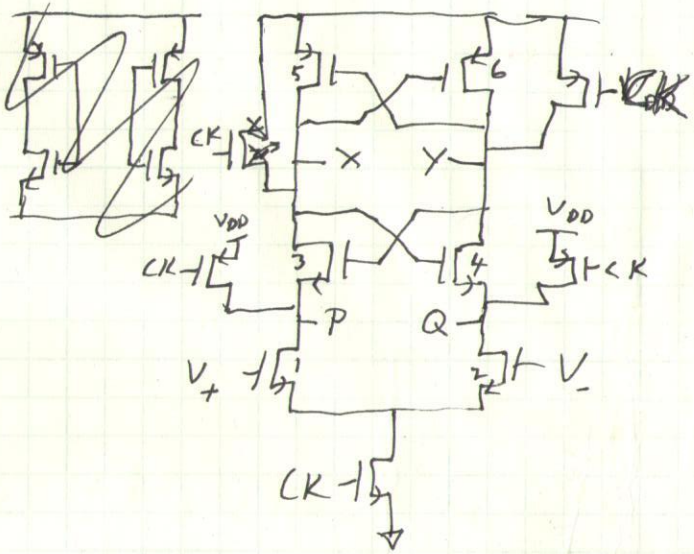
strong ARM clocked comparator
- faster
- lower power

Core element: cross-coupled inverter latch
- positive feedback
- bistable - poles in RHP real
- memory element in SRAM

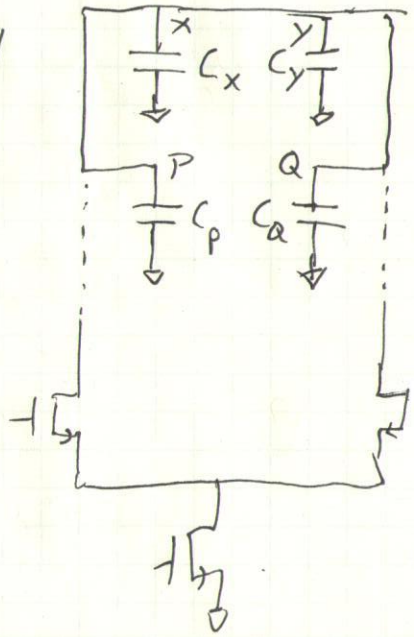




- fast $e^{t/\tau}$ $\tau = \frac{1}{\omega_n} = \frac{C_L}{g_m}$



Phase 1



Phase 2