HW1

HW2

Device Models

Diode

BJT – still popular
– good model for FETs in sub-V_t

FETs
Quadratic
sub-V_t
velocity saturated

Drift = Diffusion
Einstein Relation } $\varphi_0 = V_{TH} \ln \frac{N_A N_D}{n_i^2}$

$= V_{TH}\left(\ln \frac{N_A}{n_i} + \ln \frac{N_D}{n_i}\right)$

$n_i \simeq 10^{10} \frac{ehp}{cc}$ @ room temp.

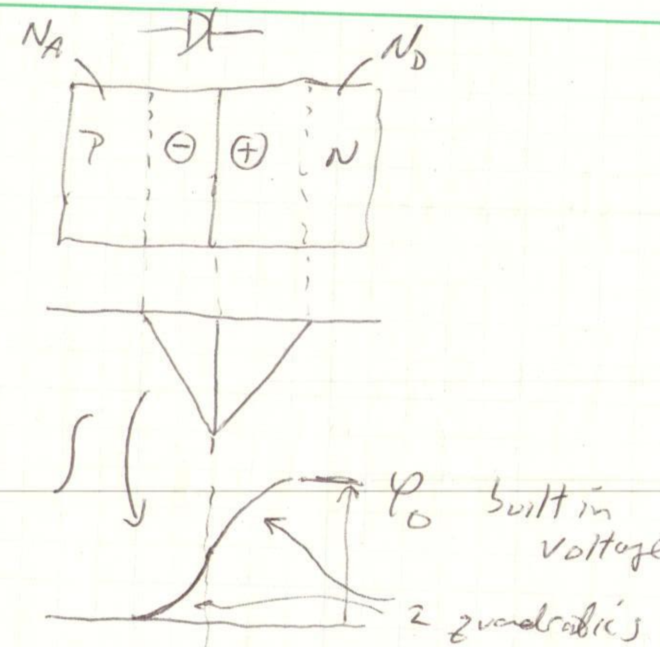
N_A, N_D in powers of 10: $10^{x+10}, 10^{y+10}$

so $\varphi_0 = V_{TH}(x \ln 10 + y \ln 10)$

$= \underbrace{V_{TH} \ln 10}_{60mV} (x+y)$ @ room temp.

Remember!

Diode

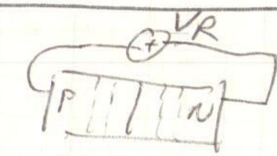


abrupt junction (rare)

Gauss:
$\int E \cdot ds = \frac{Q}{\epsilon}$

$V = -\int E \cdot dl$

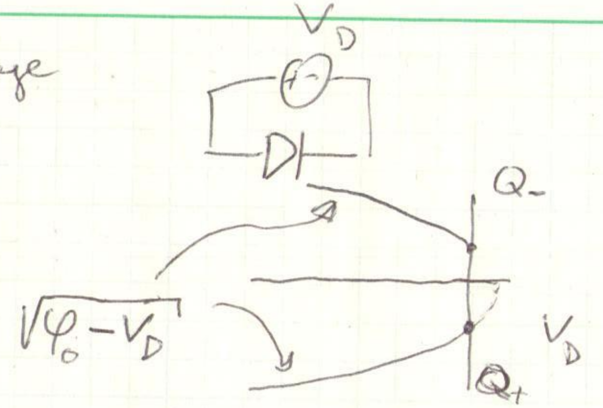
Reverse bias



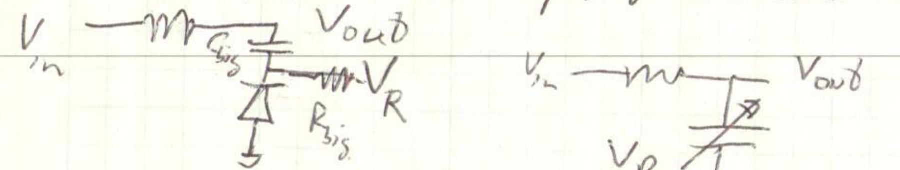
a linear increase in depletion width
gives linear increase in total charge per side
" " in peak field
which gives a quadratic increase in junction potential
$\varphi_0 + V_R$

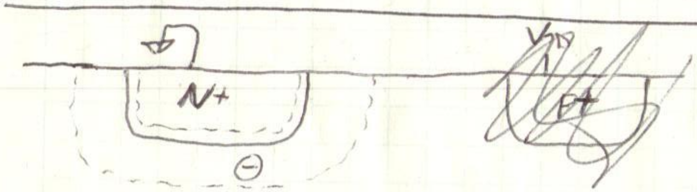
so field, charge, and depletion width all change as $\sqrt{\varphi + V_R} = \sqrt{\varphi_0 - V_D}$

charge vs voltage



What is the effective capacitance that I see?





P-biased w/ V_D

when $V_D < 0$, current is from minority carriers near depletion region getting sucked across

≈ constant w/ reverse bias

when $V_D > 0$, barrier is lowered, majority carriers flood into depl. region, become minority carriers on far side, recombine

$I_D \approx I_s\left(e^{V_D/V_{TH}} - 1\right)$

$C_j = \frac{dQ}{dV_R} = \frac{C_{j0}}{\sqrt{1 + V_R/\varphi_0}}$ ← not exactly $\sqrt{\ }$ depends on junction doping profile

OK in fwd bias to $\approx \frac{\varphi_0}{2}$

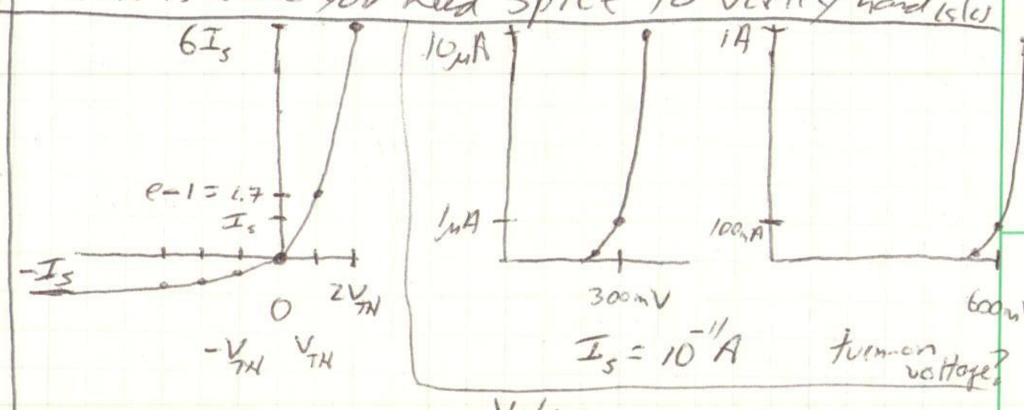
~~what if V_{out} ...~~

if V_{out} variation $<< \varphi_0$, looks like a ≈ constant variable capacitor.

if V_{out} varies ~ φ_0 ⇒ nonlinear ODE

$V_R = IR \quad I = \frac{d}{dt}(CV_c) = \frac{dC(V_c)}{dt} V_c + C(V_c)\frac{dV_c}{dt}$

this is where you need spice to verify hand calcs



Above $3V_{TH}$ $I_D \approx I_s e^{V_D/V_{TH}}$

increase V_D by V_{TH} $\quad I_D \uparrow 2.7$

increase V_D by $V_{TH} \ln 10$ $\quad I_D \uparrow 10\times$

≈60mV