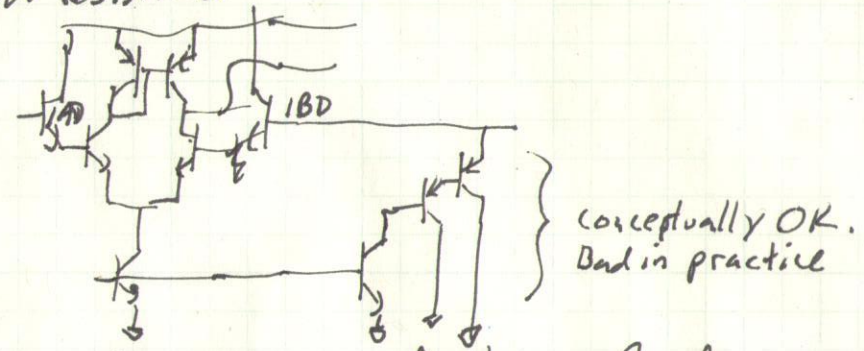
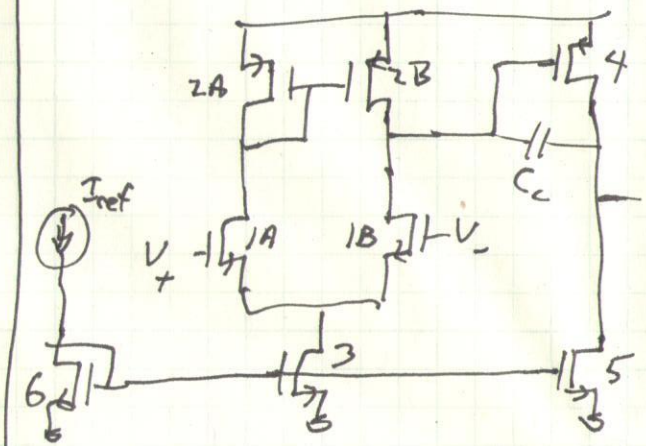
CMOS version

input resistance



Even better: measure input current and subtract it out

CMOS version - 2 stage (workhorse)

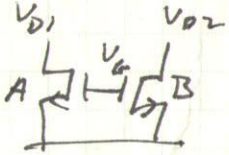


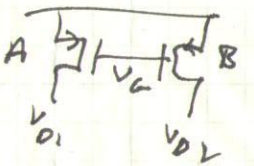
I_{ref}:  initially

typically no output stage

Diff pair	1AB	differential gain
Active load	2AB	common mode gain
gain stage	4, 5	input offset
bias network	3, 5, 6	input common mode range. output swing
signal path	1, 2, 4	frequency response
		power supply rejection
		noise
		current drive
		slew rate

current mirrors





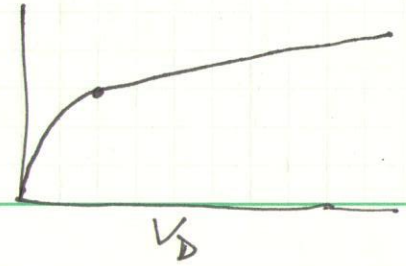
if A and B have
Same $\frac{W}{L}$, V_t, μC_{ox}
and $\lambda = 0$ how different can the currents be if both are in saturation?

A: not at all different

What if $\lambda \neq 0$?

$$\frac{\Delta I_D}{I_{DAB}} = \lambda \Delta V_D$$

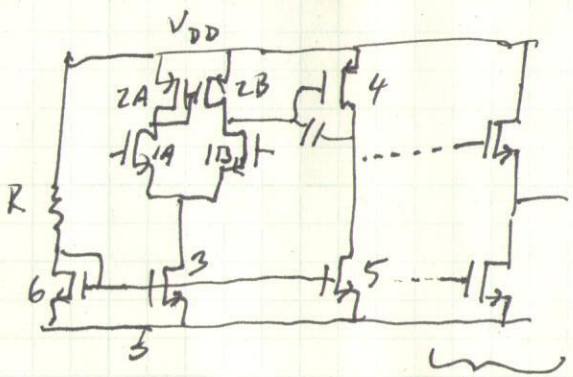
$$= \frac{\Delta V_D}{V_A}$$



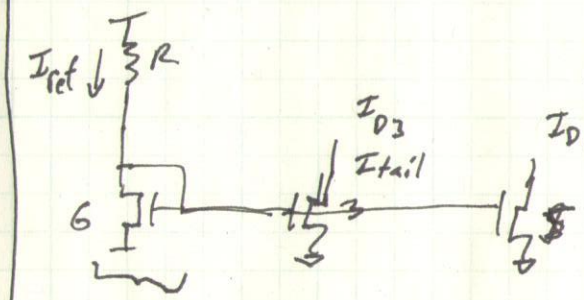
CMOS op-amp

bias network
current mirrors

feedback
& stability



Bias network



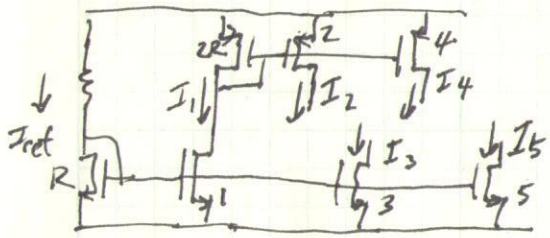
establishes V_{GS6} to pass I_{ref} w/ $(\frac{W}{L})_6$

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_t)^2 (1 + \lambda V_{DS})$$

same for all — possibly different

If you need sources & sinks (like on homework)

then mirror the current to opposite supply



$$I_1 = I_{ref} \frac{(W/L)_1}{(W/L)_R}$$

$$I_2 = I_1 \frac{(W/L)_2}{(W/L)_{2R}}$$

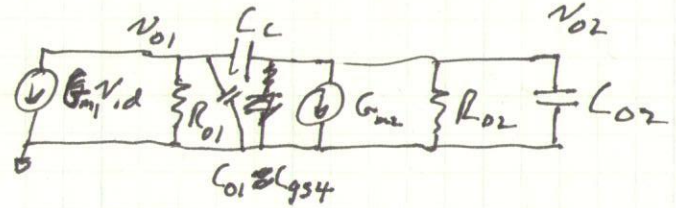
$$I_4 = I_1 \frac{(W/L)_4}{(W/L)_{2R}}$$

Always use integer ratios (literally just n copies) in transistor sizing

Always use the same L (easy, if you obey)

1st stage $G_{m1} = g_{m1a} = g_{m1b}$ $A_{V1} = \frac{g_{m1} r_{O12}}{2}$

$R_{O1} = r_{O1B} \| r_{O2B}$



2nd stage

$G_{m2} = g_{m4}$ $A_{V2} = \frac{g_{m4} r_{O45}}{2}$

$R_{O2} = r_{O4} \| r_{O5}$

if $C_L = 0$ (impossible) $\omega_{p1} = \frac{1}{R_{O1} C_{O1}}$ $\omega_{p2} = \frac{1}{R_{O2} C_{O2}}$

Why use feedback?

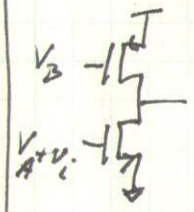
stable gain based on ratios of passive component values

improved input/output impedance

reduced nonlinearities

etc.

How do you get a gain of, say, 100? ± 1%?



design so that $g_m r_o = 100$

but these models are terrible

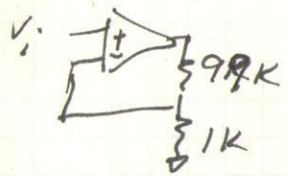
output resistance varies w/ V_o

g_m varies w/ V_o

everything varies w/ Temp, Process and supply voltage

not possible

op-amp

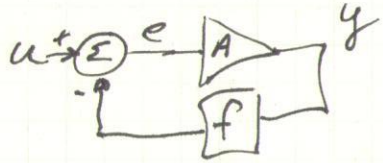


$V_o = 100 V_i$ but how accurate?

Resistor & capacitor matching pretty good ~0.1%

How much gain do we need to get 0.1% accuracy?

EE128 view



$y = Ae$

$= A(u - fy)$

$= Au - Afy$

$(1 + Af)y = Au$

$H(s) = \frac{y}{u} = \frac{A}{1+Af} = \frac{A}{Af} \frac{1}{1+\frac{1}{Af}} \simeq \frac{1}{f}\left(1 - \frac{1}{Af}\right)$

$\simeq \frac{1}{f}$ if $Af >> 1$

$\frac{1}{Af}$ ↑ gain error

need $\frac{1}{Af}$ < gain error spec, e.g. 0.1%