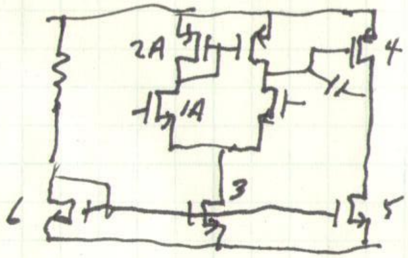
CMOS op-amps

common mode & diff mode

gain

I/O range

device sizing.



$V_{cm} = \frac{V_+ + V_-}{2}$

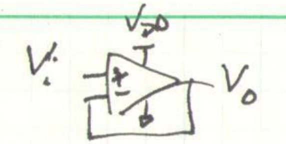
$V_{dm} = V_+ - V_-$

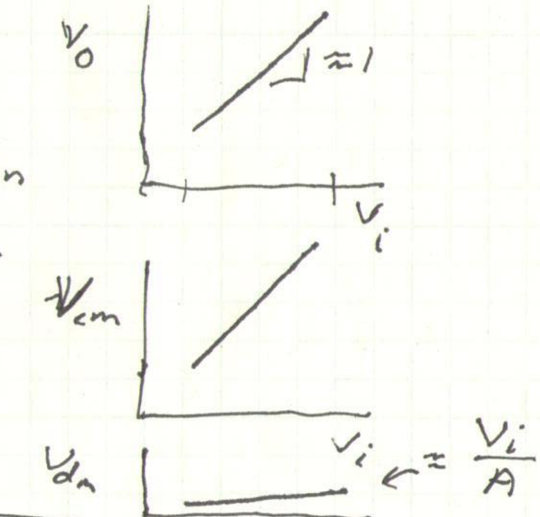
A - op-amp gain

A_{CL} - closed loop gain

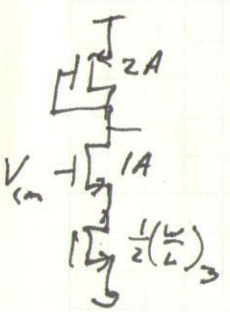
$T = Af$ = loop gain

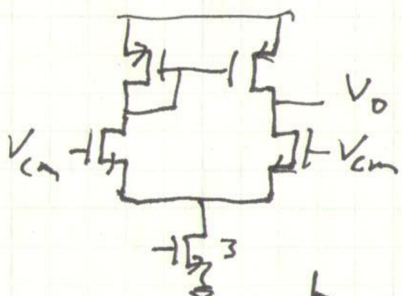
$A_{CL} = \frac{1}{1+Af} = \frac{1}{1+T}$

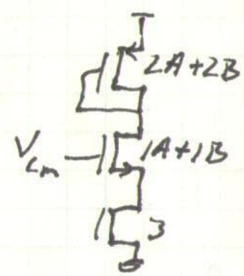


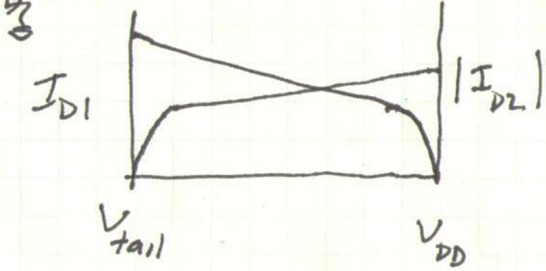


common mode gain





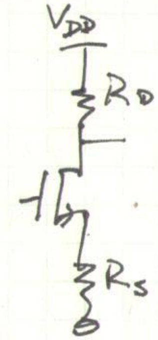




if $V_{GS1A} = V_{GS1B}$

and $V_{GS2A} = V_{GS2B}$

must have $V_{DSA} = V_{DSB}$



$G_m = \frac{g_m}{1 + g_m R_S} = \frac{1}{R_S}$ if $R_S \gg \frac{1}{g_m}$

$R_o = R_D \parallel g_m r_o R_S = R_S$ if $R_D \ll$

in our case $R_S = 2r_{o3}$ $R_D = \frac{1}{g_{m2A}}$

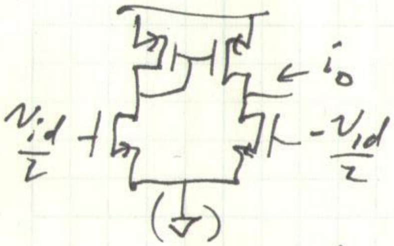
$A_V = -\frac{R_D}{R_S} = \frac{1}{2 g_{m2A} r_{o3}}$

or

$R_S = r_{o3}$ $R_D = \frac{1}{2 g_{m2A}}$ A_V same

Differential gain

easy, using <u>false</u> assumption: V_{tail} is virtual gnd



$$G_m = \left.\frac{i_o}{v_{id}}\right|_{v_o=0}$$

$$i_o = i_{d1B} + i_{d2B}$$

$$i_{d1B} = g_{m1B}\left(-\frac{v_{id}}{2}\right)$$

$$i_{d2B} = g_{m2B}\, v_{gs2B}$$

$$v_{s2B} = A_{VLEFT}\frac{v_{id}}{2} = -g_{m1A}\frac{1}{g_{m2A}}\frac{v_{id}}{2}\ \cancel{\frac{v_{id}}{2}}$$

$$i_o = -g_{m1B}\frac{v_{id}}{2} - g_{m1A}\left(\frac{g_{m2B}}{g_{m2A}}\right)\frac{v_{id}}{2}$$

$$\simeq -g_{m1}\, v_{id} \qquad G_m = -g_{m1}$$

$$R_o = r_{o1B} \| r_{o2B}$$

$$A_v = -G_m R_o = g_{m1}(r_{o1}\|r_{o2})$$

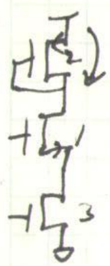
common mode rejection ratio $\frac{A_{v\,diff}}{A_{v\,common}}$

$$= g_{m1}(r_{o1}\|r_{o2})(2 g_{m2} r_{o3})$$

for two stage, both common mode <u>and</u> differential mode increase by A_{v2}

so CMRR stays the same.

Input common mode range

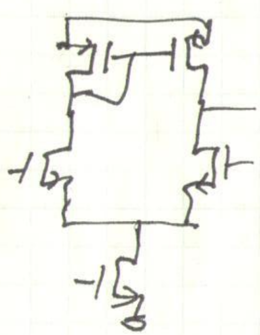


$V_{tp} + V_{ov2}$

$$V_{cm,min} = V_{ov3} + V_{tn} + V_{ov1}$$

$$V_{cm,max} = V_{DD} - |V_{tp}| - |V_{ov2}| + V_{tn}$$

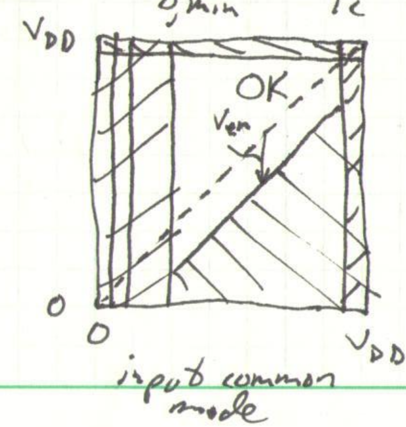
output swing, single stage



output swing

$$V_{o,max} = V_{DD} - |V_{ov2}|$$

$$V_{o,min} = V_{ic} - V_{tn}$$

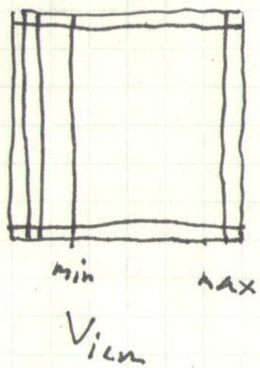


sizing

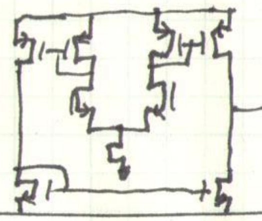
2 stage input common mode : same as single stage.

2 stage output swing : independent of input common mode

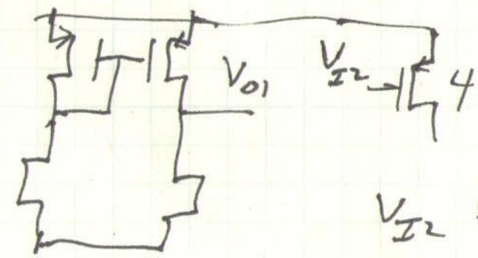
good.



current mirror op-amp is a single stage w/ same I/O range as 2 stage



2 stage bias/sizing



V_{I2} bias pt

$V_{DD} - |V_{tp}| - |V_{ov4}|$

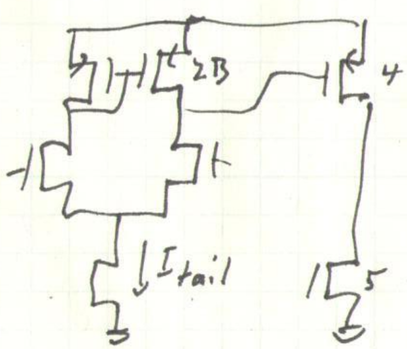
V_{O1} bias pt

$V_{DD} - |V_{tp}| - |V_{ov2}|$

//

How to set $|V_{ov4}| = |V_{ov2}|$?

if $\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_5$ then $|I_{D4}| = I_{D5} = I_{tail}$



$I_{D4} = I_{D2A} + I_{D2B}$

so $\left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_{2A} + \left(\frac{W}{L}\right)_{2B}$

$= 2\left(\frac{W}{L}\right)_2$

if $\left(\frac{W}{L}\right)_3 \neq \left(\frac{W}{L}\right)_5$ need to scale appropriately

$$\left(\frac{W}{L}\right)_4 = 2\left(\frac{W}{L}\right)_2 \frac{(W/L)_5}{(W/L)_3}$$

Specs → design

output swing, input cm ⇒ V_{ov} constraints

sink/source current ⇒ output transistor current or N/P type

(A_v, ω_u, etc)

in general, minimize power unless otherwise indic

then minimize size, capacitance