LAB REPORT 1

Due: Tuesday, Dec. 2, 2014, 8:00 a.m. in the EE 143 homework box near 140 Cory

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Total Points = 110 possible (graded out of 100)

Please be sure to include the requirement signature regarding academic honesty. All lab group members should print out this page, sign on the attached form, and include it with your Lab Report. Thank you!

REPORTS MUST BE WORD PROCESSED (EXCEPT FOR SKETCHES AND HAND WRITTEN CALCULATIONS)

Each group of students will submit one joint report. There will be a 20 PAGE max limit on the report. Profiles & Layout and Calculations do not count towards this page limit. *FOLLOW THE ATTACHED TEMPLATE FORMAT FOR THE REPORT. STUDENTS NOT FOLLOWING THIS FORMAT WILL BE DEDUCTED 10% PER SECTION DEVIATING FROM TEMPLATE.* When possible, be concise and use structured bullet points!

I. Profiles & Layout (14 Points)

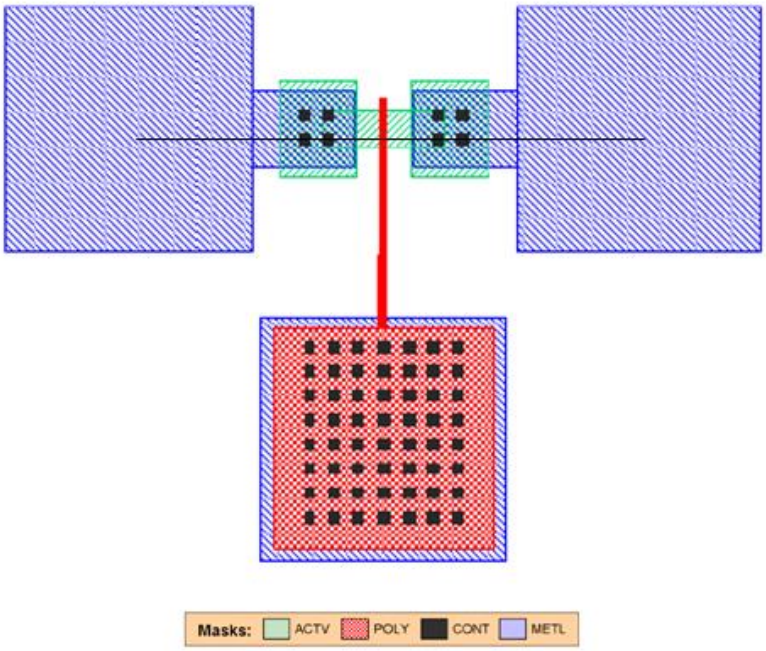
Draw cross-sectional profiles of a *MOSFET* (test structure 8) after each of the steps:

W1: Staring Wafer
W2: Field Oxidation
W3: ACTV Photolithography and Etch
W4: Gate Oxidation
W5a: Anchor Opening Photolithography for MEMS
W5b: Polysilicon CVD
W6: POLY Lithography and Etch, Source/Drain Clear
W7a: Spin-on Glass + Source/Drain Pre-diffusion
W7b: Source/Drain Drive-in + Intermediate Oxidation
W8: CONT Photolithography and Etch
W9: Aluminum Evaporation
W10: METL Photolithography + Etch
W11: MEMS Comb-drive Structure Release Photolithography + Etch

Indicate all layers. Label each feature and indicate thicknesses (make roughly proportional sketches). Illustrate and describe important details:

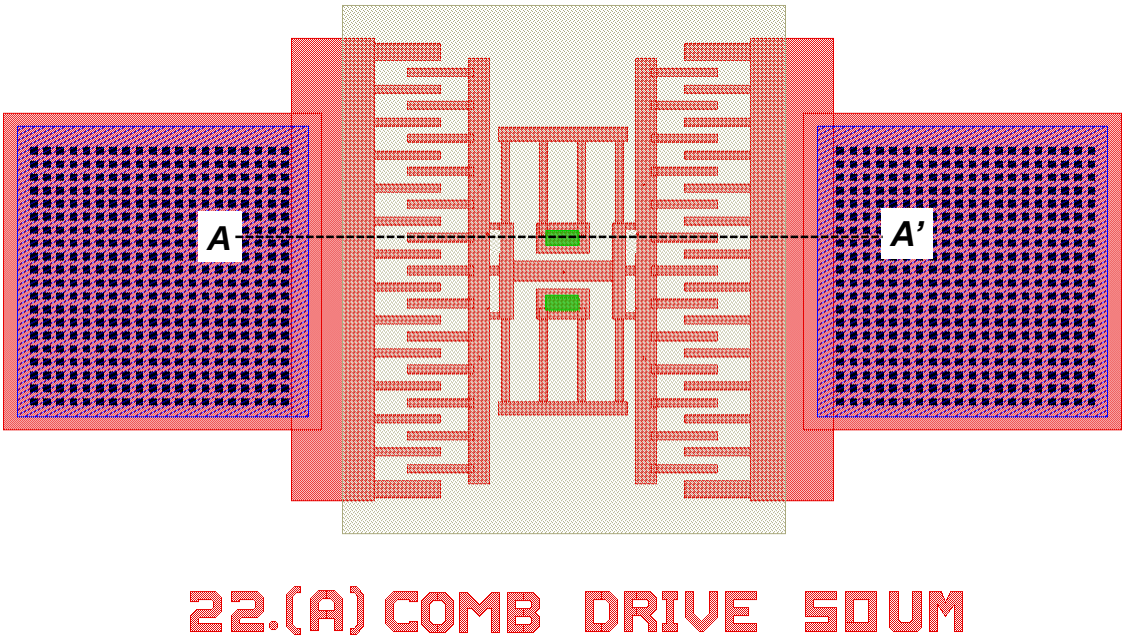
- non-planar interfaces from thermal oxidation
- isotropic etch profiles
- point-source Al evaporation
- thermal oxidation growth

These drawings should have significantly more detail than those on the lab manual website. See the diagram below for the exact cross-sections in question. (5 Points)



B. Draw top views of the same thin-oxide *MOSFET* (test structure 8) after each of the four photolithography steps. [ACTV, POLY, CONT, METL] (4 Points)

C. Draw cross-sectional profiles of the comb-drive (*MEMS* - test structure 22) after each of the 12 major processing steps, in the same fashion that you did for the MOSFET. See the diagram below for the exact cross-sections in question. The line runs through the anchor hole of the polystructure. (5 Points)



II. Process Procedures (20 Points) [Refer to Template at the back of the Report]

A. Describe monitoring measurements that were done during processing:

Film color
Line Width
Thickness
Resistivity
Vernier

Determine whether each layer was overetched or underetched? Did you purposely over/underetch? Why?

Describe how the verniers are used to measure misalignment. Using diagrams may help. Were any layers misaligned intentionally? For each pair of verniers (ACTV-POLY, ACTV-CONT, POLY-CONT, CONT-METL), describe how far the marks may be misaligned in terms of device function. (6 Points)

B. List and concisely describe the possible problems that could have occurred during the batch fabrication steps:

W2: Field Oxidation
W4: Gate Oxidation
W5: Poly Deposition
W7a: Source-Drain Prediffusion
W7b: Drive-In & Intermediate Oxidation
W9: Aluminum Evaporation
W10: Sintering

What were the sources of the problems, and how could you avoid them? How do you expect these deviations to affect the performance/function and cross-section of the device? List the types of monitoring measurements from Part A taken during each step (7 Points)

C. Other than the problems that occurred during the batch sessions, what were the particular problems (or deviations from other groups) that could occur in YOUR wafer? Specifically these are the steps where all wafers were run in individually.

W3: ACTV Photolithography
W6: POLY Photolithography
W7: SOG Deposition & SOG Strip
W8: CONT Photolithography
W10: METL Photolithography

What were the causes and how were the problems overcome? How would these affect device performance? Include any illustrations that would be helpful. List the types of measurements from Part A taken during each step (7 Points)

III. Calculations (36 Points) [Refer to Report Template at Back of Report]

Fill the template table with the following parameters from your own wafer: (3 points)

a) Film thickness (each layer)
b) Sheet Resistance (after ion implantation and S&D formation)
c) % over/underetch measured photoresist from theoretical (each layer)

Calculate the parameters asked for in the following questions—list both the theoretical values and the empirical values, when applicable. We would like to see that you understand what processing abnormalities may have led to a discrepancy between the two. Neatly write up and annotate all calculations and attach in appendix. (Points will be deducted if we can not understand what you wrote).

1. Theoretical and experimental thicknesses of field oxide, gate and intermediate oxides (Include orientation dependence of oxidation rate but not impurity dependence) (9 points)
2. Junction depths after pre-diffusion and drive-in (theoretical, assume only phosphorous doping with surface concentration limited by solid solubility). You must consider the effect of the initial ion implantation. For pre-deposition you may use the box approximation, but for drive-in you must use the half-gaussian calculation. Why is this? (10 points)

3. Final surface concentrations of dopants, as determined from Irvin's curves using sheet resistance measurements made in lab. (2 points)

4. Plot or sketch the change of dopant profile from the silicon surface through the source-drain after each thermal step.

   - Field Oxidation
   - Gate Oxidation
   - Poly-Deposition
   - Pre-Deposition
   - Drive-In & Intermediate Oxidation.
   - Sintering

   Quantitatively label significant points such as Peak concentration, Peak Width, Junction Depth. Show movement of the Silicon-Silicon Dioxide interface and qualitatively show non-ideal effects such as dopant redistribution during oxidation. (11 points)
5. Lateral diffusion under the MOSFET gates. You may estimate. Justify estimation. (Theoretical). (2 points)
6. List an estimate of the Young's modulus, Poisson ratio, and coefficient of thermal expansion for SiO_2, poly-Si, and Al films as deposited. (You can find these in a table in many physics/ME textbooks, or in a web-based search.) (2 points)

IV. Questions (30 Points - 2 points each) (3 Page Limit)

Answer these questions in the most concise manner possible. A few lines should suffice for each.

1. What type of photoresist (positive or negative? I-line or G-line?) do we use in the lab? What do I-line and G-line refer to? Briefly describe how the resist responds to the process steps like spinning, UV light exposure and development.
2. What is the purpose of baking the wafers at 120 °C before depositing HMDS? What is the purpose of the 90 °C bake after spinning on photoresist? What happens if the soft bake is too hot and too long (say 120 °C, 5 minutes)?

3. What is the purpose of hard bake? What happens if we skip this step? What may happen if the bake is done at a temperature above 120 °C (say 200 °C)?
4. We do lithography steps under yellow light only. What is the consequence if we expose the wafers to fluorescent light before development? What if we expose them to fluorescent light after development? Would red light damage your process?
5. What are the differences between wet and dry oxidation that lead us to use one for the gate oxide and one for the field/intermediate oxide? What is the purpose of annealing in nitrogen after oxidation?
6. How do you determine etching time using theoretical etch rate in literature? List two ways to determine etch time empirically from lab measurements, when you etch the layers. (Hint: these methods include visual cues.). How close are the experimental and the theoretically calculated values?
7. Before n+ deposition (prior to SOG spinning), we clean in Piranha but not in HF. Before gate oxidation, we clean in both. Why the difference?
8. Why is 5:1 BHF (5:1 NH_4F:HF) used for etching features in the oxide while 10:1 BHF is used for cleaning and spin-on-glass stripping? Why buffered HF?
9. What would happen if we skipped the HF dip before metallization?
10. What is etch selectivity?
11. Why do we first use the roughing pump and then the diffusion pump when pumping down the aluminum deposition system? Why must the foreline pressure be kept below 100 mTorr?
12. What is the Al etchant composed of? What happens if you use it at room temperature? What is the purpose of sintering? What will result if sintering step is skipped? What happens if sintering temperature is too hot or too low?
13. Briefly explain the mechanism of XeF_2 etching. Is the etch isotropic or anisotropic? In an integrated CMOS/MEMS process, is there any consequence to using KOH instead of XeF_2 for etch?
14. What would happen if a thick oxide film was left on the wafers as it went into the XeF_2 etching step?
15. Identify two of the 11 major processing steps that are unnecessary to fabricate a functional oxide cantilever beam. Why are they unnecessary?

V. Bonus Questions (up to 10 Points)

1. Simulate the 143 process flow in Tsuprem4 [8 points] ← (updated on 11/20/14, you only need to simulate the NMOS LDD example available online (i.e., s4ex4a, -b, -c.inp))
2. Describe an alternate method for doing one of the process steps (i.e. LOCOS instead of Field Oxide, Sputtering instead of Evaporation, etc) and the tradeoffs.

Lab Report Template:

I. Profiles & Layout:

A. Thin oxide MOSFET Cross Section

B. Top Views

C. Comb-drive MEMS Structure Cross Section

II. Process Procedures:

A. Process Monitoring Measurements
- Measurement Type and Description
- Over-Etch/Under-Etch
- Misalignment Tolerance

B& C. Batch and Individual Processing Steps:

Week 2: Field Oxidation:
- Batch Processing Problems
- Measurements Taken

Week 3: Field Oxide Cut
- Individual Processing Problems
- Measurements Taken

Week 4: Gate Oxidation
- Batch Processing Problems
- Measurements

Week 5: Poly Deposition
- Batch Processing Problems
- Measurements

Week 6: Gate Definition
- Individual Processing Problems
- Measurements

Week 7: S/D Diffusion and Intermediate Oxidation
- Batch Processing Problems
- Individual Processing Problems
- Measurements

Week 8: Contact Hole Cut
- Individual Processing Problems

- Measurements

Week 9: Metallization
- Batch Processing Problems
- Measurements

Week 10: Metal Definition
- Batch Processing Problems
- Individual Processing Problems
- Measurements

Week 11: MEMS Structure Release
- Individual Processing Problems
- Measurements

III. Calculations:

IV. Questions:

V. Bonus:

VI. Appendix:

Calculations Results Template:

Film Thicknesses: (**note: Not all lab sections took Linewidths after PR strip, those may skip that column**)

Layer	Theoretical Calculation	Experimental	% Error	Linewidths (Photoresist)	Linewidths (after PR Strip)	% Overetch
Field Oxide						
Polysilicon						
Gate Oxide						
Intermed Oxide						
Aluminum						

Overetch:

Layer	Measured Linewidth	% Overetch	Theoretical Etch Time	Actual Etch Time	% Overetch
Field Oxide					
Polysilicon					
Gate Oxide					
Intermed Oxide					
Aluminum					

Sheet Resistance:

Layer	Sheet Resistance	Surface Concentration (Calculated)
ACTV After Field Oxidation		
Polysilicon		
ACTV After Pre-Dep		
ACTV After Drive-in		
METL		

Theoretical Junction Depth

Layer	Vertical Junction Depth	Lateral Junction Depth
ACTV After Pre-Dep		
ACTV After Drive-in		

EECS 143 Lab Report 1

Fall 2014

In signing below, I attest to the fact that I have read and have adhered to the policies and guidelines discussed in the EECS Departmental Policy on Academic Dishonesty, as found at: http://www.eecs.berkeley.edu/Policies/acad.dis.shtml

Name: _____

Signature: _____

Date:_____

Name: _____

Signature: _____

Date:_____

Name: _____

Signature: _____

Date:_____