LAB REPORT 2

***Due: Friday, Dec. 12, 2014*, 8:00 a.m. in the EE 143 homework box in 140 Cory**

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Total Points = 115 possible

Please be sure to include the requirement signature regarding academic honesty. All lab group members should print out this page (the last page after the report template), sign on the attached form, and include it with your Lab Report.

REPORTS MUST BE WORD PROCESSED (EXCEPT FOR SKETCHES AND HAND WRITTEN CALCULATIONS)

EVERY GROUP WILL SUBMIT ONE JOINT REPORT. FOLLOW THE TEMPLATE FORMAT FOR THE REPORT. STUDENTS NOT FOLLOWING THIS FORMAT WILL BE DEDUCTED 10% PER SECTION DEVIATING FROM TEMPLATE.

I. Introduction

This report will summarize characterization of your test structures. The two purposes of characterization are to teach you how to use the equipment and techniques common to semiconductor device analysis, and to compare the actual behavior of your devices with that predicted theoretically. Each group of two (or three) students will submit one joint report. Please follow the outline given in the table of contents above, which will allow the TAs to grade the reports clearly based on the within-section point values described below.

Working vs. Non-working devices

We understand that some of your devices may not work for a variety of reasons. If this is the case for your group, you are allowed to borrow a wafer from other groups to get functioning device characteristics. However, if your devices do not display precisely the same characteristics as shown in the "Device Characterization" link, do not panic. Keep in mind that the point of this lab report is for you to compare your results to the reference and explore which fabrication steps might have caused that problem. If particular devices do not work in your entire lab section's wafers, please talk to your TA about the procedure to proceed with the parameter extractions and discussions for this report.

II. Measurements and Parameter Extraction (50 points)

In this section, you are asked to **draw the measurement setup diagrams**, **plot the measured data,** and **extract parameters from the measured data,** for each of the major device types. Among the structures and devices to be measured are line width test patterns, resistors [2a, 2b], four-point contact resistors [17a, 17b], contact-chain resistors [2c, 2d], diodes [7], MOSFETs [8-10], inverters [14], and capacitors [3-5].

In making these measurements, you should consult the "Device Characterization" and "Characterization Schemes" links on the EE143 website. The "Device Characterization" link provides background, theory, and equations associated with the measurements in question, while the "Characterization Schemes" link presents the specific measurement setups required.

1. Measurement Setups

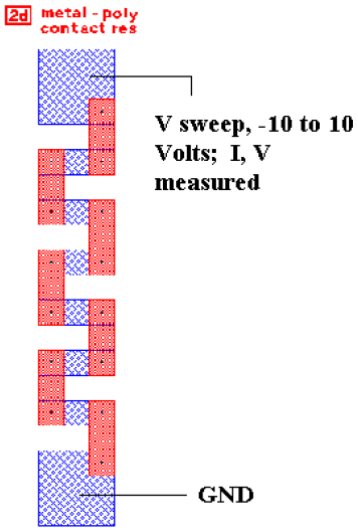
For each structure or device to be measured, draw a diagram that describes the measurement setup, including:

(1) A top down picture of the device.

(2) A brief description of what stimuli were applied and what measurements were taken at each of the contact pads.

Note that the measurement setups to be used will generally mimic those on the "Characterization Schemes" page (on the EE143 website), except for deviations explicitly specified in the next section on data measurements. Also, note that MOSFETs will require at least two measurement setup diagrams, one for I_D-V_{DS}, and one for I_D-V_{GS}; and diodes will require two diagrams, one for forward bias and one for reverse bias.

As an example, the measurement setup for a metal-to-poly contact-chain resistor would look as follows:



2. Data Collection and Parameter Extraction

1) Line width/Misalignment

- Measure the line widths on the test patterns for each lithography step and create a table of all the line widths using the format in the Lab#2 template.
- Measure the misalignment incurred for each lithography step. Use the alignment verniers for precision.

(Note that this section can basically be copied over from lab report 1, if a thorough job was done for that report.)

2) Four-Point Resistors [2a, 2b]

- Plot I_{S1} vs. V_{DIF} for each device. (total of 2 plots) Note that V_{DIF} is defined as the difference between the two measured voltage values on S1P and S2P in the "Characterization Schemes" page (on the EE143 website).
- Extract the resistance of each device.
- Use the final measured line width data (and thus, the overetch/underetch data) from the above problem to calculate the actual dimensions of each resistor. Then, calculate the sheet resistance for each structure.
- For the diffusion resistor [2a], use the junction depth value calculated in Lab Report 1 to determine the surface doping concentration, N_D, and electron mobility (see Appendix for reference).
- Using the poly resistor [2b], calculate the polysilicon resistivity in (ohm-cm).

3) Four-Point Contact Resistors [17a, 17b]

- Plot I_{S1} vs. V_{DIF} for each device. (total of 2 plots) (same setup as for 2a and 2b resistors)

- Extract the contact resistance of each device.

4) Contact-Chain Resistors [2c,2d]

- Plot I_{S1} vs. V_{DIF} for each device. (total of 2 plots)
- Extract the resistance of each structure.
- Calculate the contact resistance for the contacts of each structure using the sheet resistance values from item 2 (four-point resistors) above.

5) Gate Oxide Capacitor [4]

- Plot *C*-*V* with lights on and off. (total of 2 plots)
- Determine the minimum capacitance, both with lights on and off.
- Measure the capacitance at $V_G = -5$ V and calculate the gate oxide thickness and the C' (capacitance / unit area).
- Calculate the maximum depletion width and the substrate doping concentration.
- Extract the flat band capacitance (C_{FB}) and the flat band voltage (V_{FB}), then calculate interface fixed charge density (Q_f).
- Report/estimate the threshold voltage V_T.

6) Field Oxide Capacitor [3]

- Plot *C*-*V*.
- Measure the capacitance in the accumulation region (close to $V_G = -5$V).
- Determine the field oxide thickness.

7) Intermediate Oxide Capacitor [5]

- Plot *C*-*V*.
- Measure the capacitance in the accumulation region (close to V_G = -5V).

8) Diode [7]

- Plot *I* vs.*V* for forward (normal) and reverse operation. (total of 2 plots)
- Extract the turn-on voltage and the series resistance.

9) MOSFETs of Varying Length [8a-d]

- Plot I_D vs.V_{DS}, V_{GS} = 0-5 V (1V steps) for each device. (total of 4 plots)
  - Estimate the channel-length modulation coefficient, λ, for each device and plot λ vs. L_{drawn}.
- Plot I_D vs. V_G, V_D = 0.05 V and V_B = 0 V for each device. (total of 4 plots)
  - Estimate V_T for each device.
  - Estimate ΔL.

- Plot V_T vs. L_{eff}.

10) MOSFETs of Varying Width [9a-c]

- Plot I_D-V_{DS}, V_G = 0-5 V (1V steps) for each device. (total of 3 plots)
- Plot I_D-V_G, V_D = 0.05 V and V_B = 0 V for each device. (total of 3 plots)
  - Estimate V_T for each device.
  - Estimate ΔW.
  - Plot V_T vs. W_{eff}.

11) Large MOSFET [10]

- Plot I_D vs. V_{DS}, V_G = 0 - 5 V (1V steps)
- Plot I_D vs. V_G, V_D = 0.05 V and V_B = −10-0 V (1V steps)
  - Determine μ_{eff} (V_G) and plot the mobility μ_{eff} vs. V_G for V_G>V_T, at V_{SB} = 0 V.
  - Determine the "low-field" mobility, μ.
  - Estimate V_T (V_{SB}) and plot V_T vs. $\sqrt{V_{SB}+0.7}$ for V_{SB} ranging from 0-10V. Explain why the curve is not a straight line.
  - Determine the body effect factor γ and N_A.
  - Plot log (I_D) vs. V_G at V_{SB} = 0 V and determine the subthreshold slope.

12) Inverter [14]

- Plot V_{in} vs. V_{out}.
- Determine V_M, where V_{in}=V_{out}.

NOTE: Label ALL plots with appropriate axes and numerical scales, and title the corresponding device names. Also, label clearly all the marks or fitting lines on the measured plots used for parameter extraction.

III. Theoretical Calculations (25 points)

1. Measured Physical Dimensions and Parameters

In this section, theoretical values should be calculated totally independent of characterization measurements specified in the section above. You should use only values from report 1. If you measured a value in report 1, use it. If not, use a calculated value. For example, you should use your earlier measured or extracted t_{ox} from the first lab report. But you did not measure junction depth X_j, surface doping concentration N_D, and lateral diffusion, so use calculated values for these.

Compile this data into a table, such as below.

Parameter	Measured Value

Field t_{ox}	
Gate t_{ox}	
Intermediate t_{ox}	
X_j	
$X_{j,\ lateral}$	
N_D	

2. Resistors [2a, 2b]

Use the thickness and/or junction depths and doping from report 1 to determine the expected theoretical sheet resistance for both 2a and 2b.

3. Contact Resistances [17a, 17b]

Consult Jaeger's section on contact resistance and report values for the theoretical contact resistances expected for devices 17a and 17b. (The contacts are $5\mu m \times 5\mu m$)

4. Contact-Chain Resistors [2c, 2d]

Calculate the expected resistance of each contact chain according to the sheet resistance and contact resistance obtained from **2** and **3**.

5. Gate/Field Oxide Capacitor [3, 4]

Describe the physics of the MOS capacitor. In particular, what does MOS mean? Discuss the three regions of an MOS capacitor. Why does the Intermediate Oxide Capacitor [5] not display MOS effects? Plot the theoretical CV curve for the Intermediate Oxide Capacitor and a gate oxide capacitor on the same plot.

Calculate the theoretical V_T and V_{FB} for the gate oxide capacitors and field oxide capacitors in your lab process and discuss the expected photoelectric effect.

6. Diode

Calculate the built-in potential (or turn-on voltage) for the *pn* junction. You can assume a step junction here.

7. MOSFETs

- MOSFETs of varying length [8] and of varying width [9]
  - Determine the ΔL and ΔW, respectively.
- Large MOSFET [10]
  - Calculate V_T (same as equations used for the MOS gate capacitor).
  - Calculate the expected value of the body factor (γ).
  - Determine the substrate concentration
  - Determine the "low-field" mobility, μ, as a function of the doping.

8. Inverter

Draw a well-labeled equivalent circuit for the inverter structure [14]. Simplify to voltage divider with variable resistors. Draw curves of output voltage V_{out} versus input voltage V_{in} with V_{DD} as a third variable.

IV. Discussion (25 points)

1. Create one master table containing all of the measured values from the parameter extraction section, all the theoretical values from the theoretical calculations section, and the percentage difference between the two. (So, three columns for each device parameter.) You can use the table below as a reference. For each of the device parameters, discuss what may have caused the discrepancy (if any) between the measured and theoretical values. Draw up this point-by-point discussion in a **numbered, organized, and concise** form. Write only several sentences per point. Be concise, but thorough. (15 points)
2. Plot ideal square law MOSFET characteristics against one of your MOSFETs [8c]. Describe the non-ideal effects that can explain the differences between the two plots. (10 points)

V. Optional Questions (15 points)

1. In the final step, we didn't successfully release the MEMS comb-drive structures. Propose reasons that might cause this problem. (5 points)
2. Simulate the 143 process flow in Tsuprem4. [Note: A short Tsuprem tutorial and the Tsuprem4 manual are online in the Lab Part II section.] (10 points)

VI. Appendix

- The majority carrier mobility versus doping at room temperature can be computed using

$$\mu = \mu_{min} + \frac{\mu_0}{1 + (N/N_{ref})^{\alpha}}$$

where values for the parameters in Si are listed in the following table:

Parameter	Electrons	Holes
N_{ref} (cm^{-3})	1.3×10^{17}	2.35×10^{17}
μ_{min} (cm^2/V-sec)	92	54.3
μ_0 (cm^2/V-sec)	1268	406.9
α	0.91	0.88