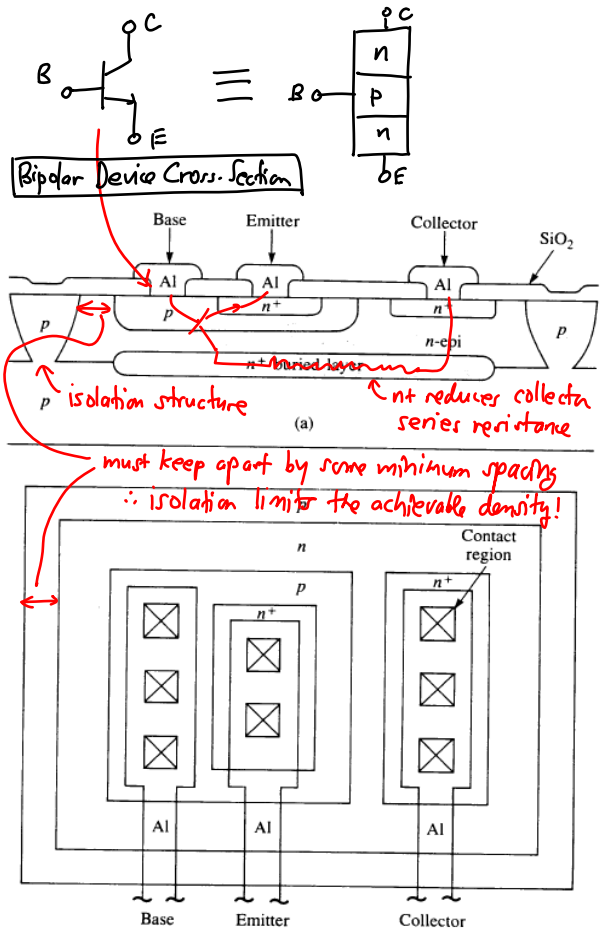
EE 143: IC History & Review of Devices 9/2/14Tu

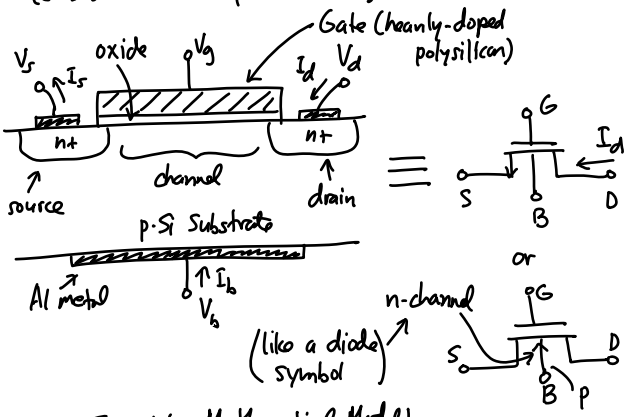
- Reading: Jaeger, Chpt. 1
- Lecture Topics:
  - History of IC's
  - Devices of Interest
    - → MOS transistor
    - → Micromechanical structure
- ----------
- History of IC's:
  - 1834: Difference Engines (mechanical computers)
    - → Gears, cranks, levers, decimal, pipelining!
  - 1904: Vacuum tube invented
    - → Yielded the ENIAC vacuum tube computer
  - 1925: J. Lilenfield proposed the MOSFET transistor
    - → Problem: knowledge of materials not sufficient to get this to work
  - (instead)
  - 1947: Invention of the transistor (Bardeen, Brattein, Shockley)
  - 1949: Invention of the Bipolar Xsistor (Shockley)
  - 1956: First digital logic gates (Harris)
  - 1959: Invention of planar silicon processing (Kilby, Noyce)
  - Then a slew of bipolar technologies



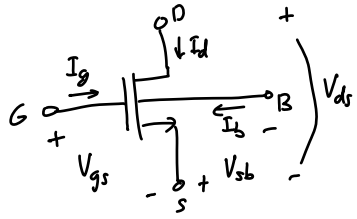
  - → TTL (1965)
  - → ECL (1967)
  - → MTL/I^2L (1972)
  - → SiGe heterostructures (1990's)
  - Bipolar ruled during the 60's and 70's, because it was faster than anything else, incl. MOS
  - But soon, its excessive power consumption caught up, and MOS began to come into favor as small channel lengths boosted the speed of MOS

Physical Structure & Device Symbols

(cross-section view of NMOS device)



NMOS Transistor Mathematical Model



① Cut-off Region: $(V_{gs} \le V_t)$

$I_g = I_b = 0$; $I_d = 0$

② Linear (or Triode) Region: $(V_{gs} - V_{tn} \ge V_{ds} \ge 0)$

$I_g = I_b = 0$; $I_d = \mu_n C_{ox} \frac{W}{L}\left(V_{gs} - V_{tn} - \frac{V_{ds}}{2}\right)V_{ds}$

$= k_n\left(V_{gs} - V_{tn} - \frac{V_{ds}}{2}\right)V_{ds}$

③ Saturation Region: $(V_{ds} \ge V_{gs} - V_{tn} \ge 0)$

$I_g = I_b = 0$; $I_d = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{tn})^2(1 + \lambda V_{ds})$

$= \frac{1}{2}k_n(V_{gs} - V_{tn})^2(1 + \lambda V_{ds})$

where: $\mu_n \triangleq$ e- mobility in the channel

$C_{ox} \triangleq$ gate oxide capacitance per unit area

$k_n = k_n' \frac{W}{L} = \mu_n C_{ox}\frac{W}{L}$

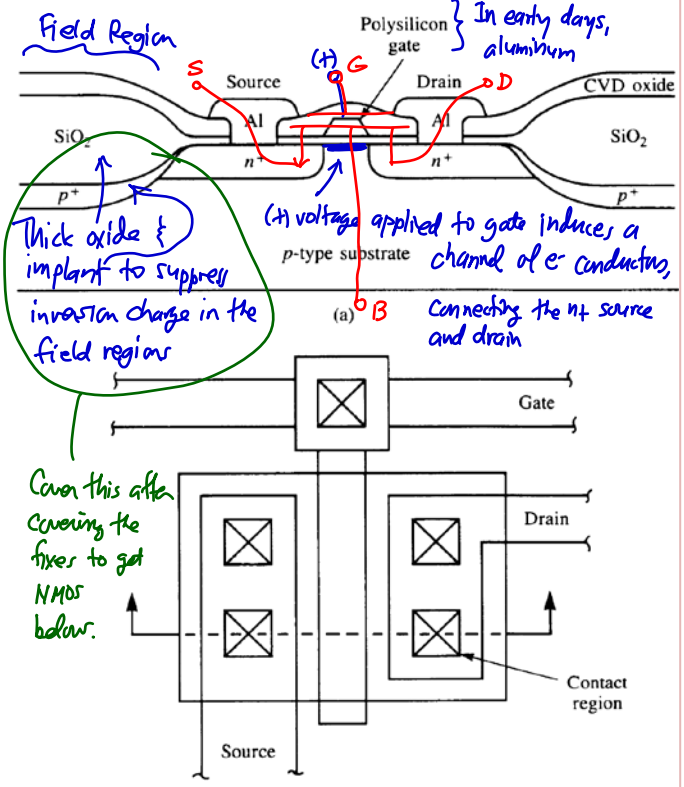
$I_g = I_b = 0$ for all regions (at least for dc)

$$V_{th} = f(V_{SB}) = V_{to} + \gamma\left(\sqrt{V_{SB} - 2|\phi_f|} - \sqrt{2|\phi_f|}\right)$$

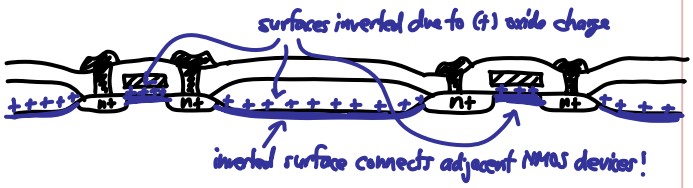
"+"

Body Factor → $\gamma = \frac{1}{C_{ox}}\sqrt{2q\epsilon_s N_{sub}}$ ← substrate doping conc.

NMOS Device Cross-Section



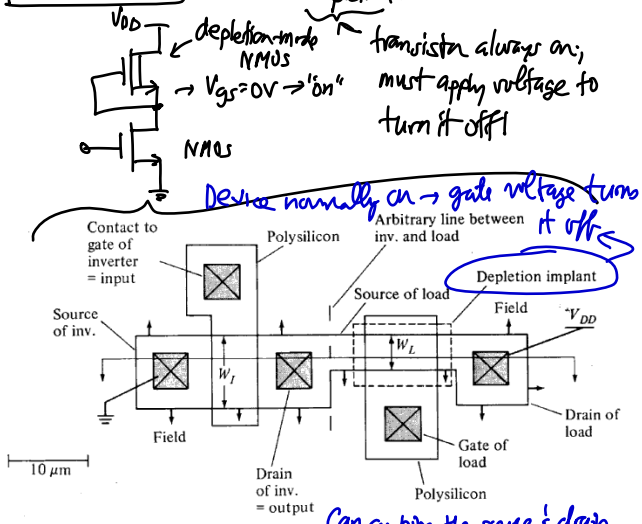
- Fairly simple process: only 5 masks; note that this is much smaller than today's proess, which might have more than 28 masking steps
- The rise of MOS occurred in steps:
- 1965: PMOS w/ Al gate
  - → Used <111> wafers because bipolar used them
  - → This forced the use of PMOS, since oxide charge was dense in <111>-Si to oxide interfaces
  - → Oxide charge made it difficult to isolate NMOS devices



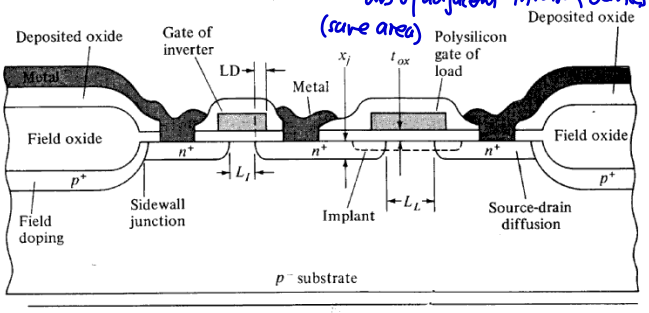
- 1967-70: Al gate NMOS
  - → Use of <100>-Si together with sintering reduced oxide charges
  - → Speed faster than PMOS and path to matching bipolar speed could be seen

- 1970: Si-gate NMOS
  - → Advantage: self-alignment of source & drain
  - → Problem: power consumption (similar to bipolar)

NMOS Inverter (1980's → depletion load

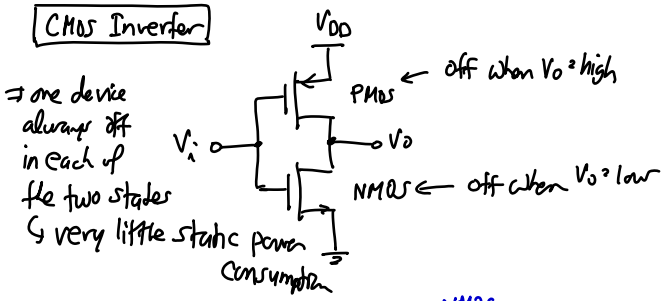


Can combine the source & drain area of adjacent inverter devices (save area)



- To reduce power consumption, a complementary device was needed
- This is where CMOS looked advantageous

CMOS Inverter



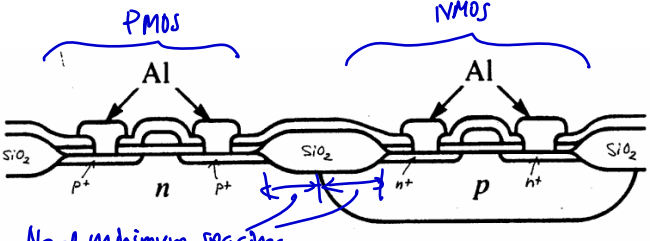
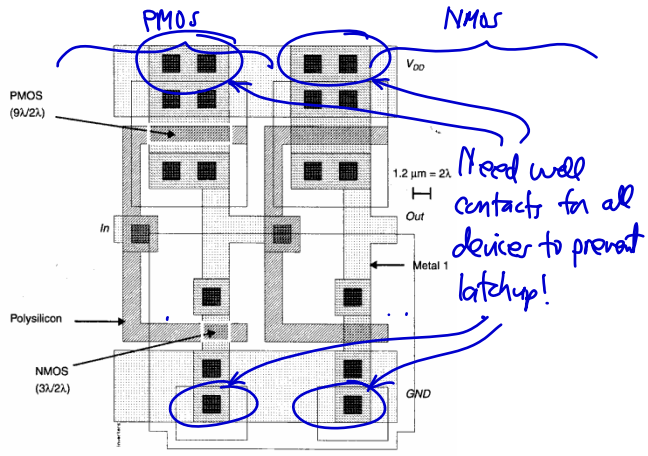
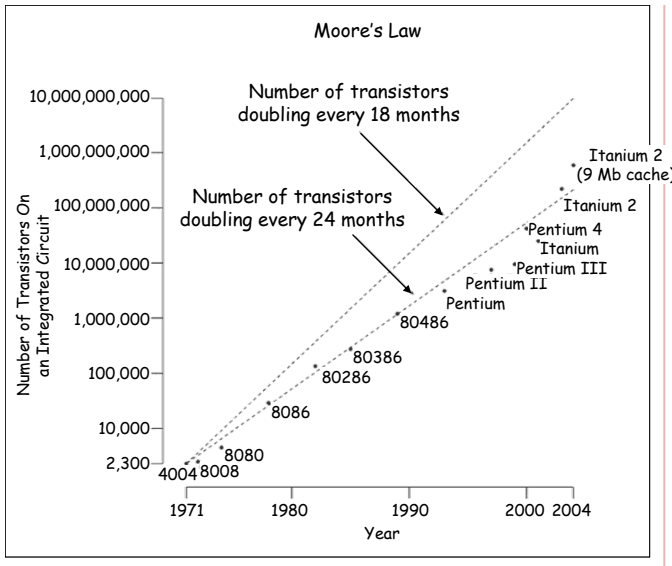


Fig. 2.1



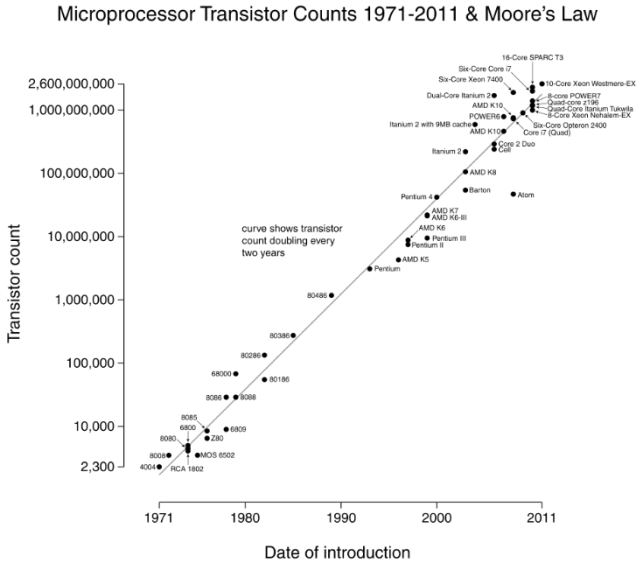
- 1963: pwell CMOS
  - → CMOS gate actually came before NMOS or PMOS, but poor control of oxide quality at the time prevented it from thriving
  - → Why didn't CMOS thrive in 1963?
    1. Higher fabrication cost.
    2. Latch-up problems.
    3. Lower packing density due to need for wells.
    4. CMOS slower than NMOS due to larger gate capacitance.
- But soon power became an issue:
- 1971: Intel 4004 4-bit microprocessor
  - → 2,300 devices (PMOS)
- 1978: Intel 8086 16-bit microprocessor
  - → 29,000 devices (NMOS); power dissipation beginning to get up there: 1.5W @ 8MHz
- 1985: Intel 80386
  - → 275,000 devices → NMOS light bulb!
  - → A low power technology was needed
- Result: CMOS takes over
  - → Intel 80C86 (CMOS version of 80386)
  - → Intel 80486: 1.2 million Xsistors
  - → Intel Pentium (P5): 3 million Xsistors
  - → Intel P6: 5.5 million Xsistors in core, 15 million more in secondary cache
  - → And of course it keeps going to today …
  - → Intel Core 2 Duo: 820 million Xsistors
  - → Intel Core i7: 1.4 billion Xsistors (in 2012)

- All of this is a result of scaling via micro (and now nano) technology

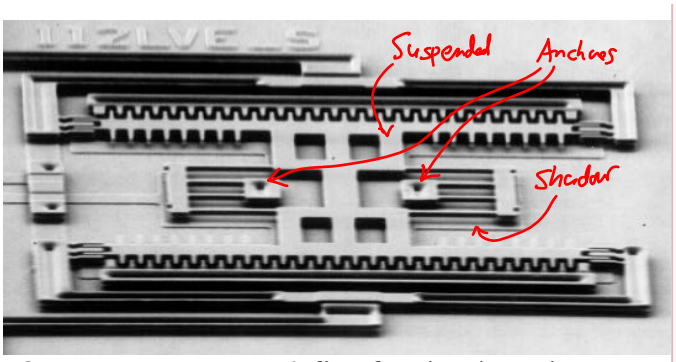


- Much of today's progress is driven by a roadmap generated many years ago

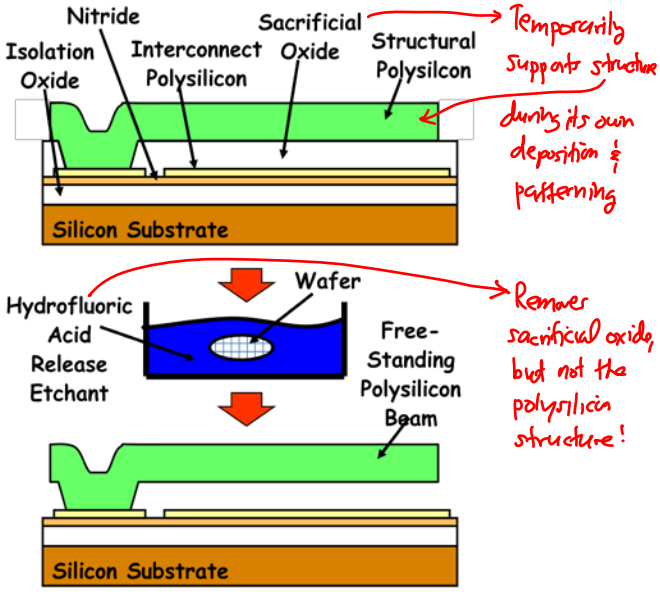
Year	1999	2002	2005	2008	2011	2014
Feature size (nm)	180	130	100	70	50	35
Logic trans/cm^2	6.2M	18M	39M	84M	180M	390M
Cost/trans (mc)	1.735	.580	.255	.110	.049	.022
#pads/chip	1867	2553	3492	4776	6532	8935
Clock (MHz)	1250	2100	3500	6000	10000	16900
Chip size (mm^2)	340	430	520	620	750	900
Wiring levels	6-7	7	7-8	8-9	9	10
Power supply (V)	1.8	1.5	1.2	0.9	0.6	0.5
High-perf pow (W)	90	130	160	170	175	183



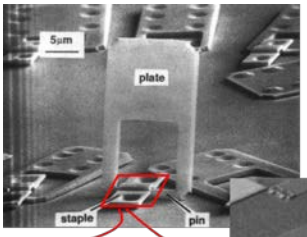
- The next jump in technological capability came with the advent of MEMS, which then led to nanotechnology
- 300 kHz Folded-Beam Micromechanical Resonator:



- Process cross-section & flow for the above device

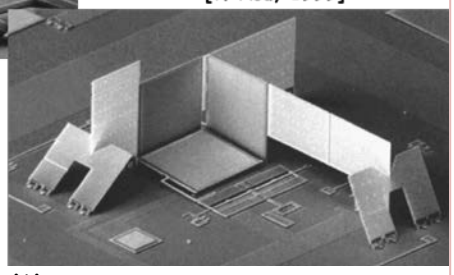


- Prof. Kris Pister's pop-up MEMS:

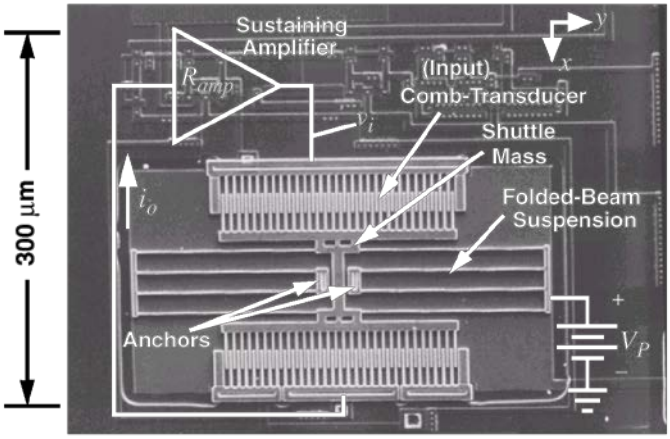


First MEMS hinge
[K. Pister, et al., 1992]

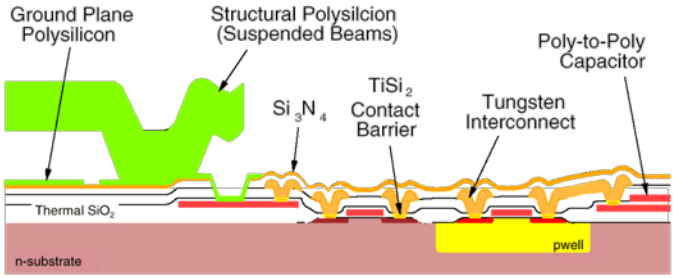
Corner Cube Reflector
[v. Hsu, 1999]



- Show video: Ming Wu
- Show video: fully integrated micromechanical resonator oscillator
- Fully integrated micromechanical resonator oscillator:



- Process cross-section for the above device
  - Full planar integration with transistors on a single-chip
  - Allows smaller size, better performance, and lower cost in many situations



- This course will focus mainly on transistor fabrication, but many of the concepts learned will be applicable to MEMS, as well
- Your lab layout introduces for the first time a MEMS structure that has a better chance of working than previous renditions of this class