Advanced Isolation

But in reality, topography will greatly limit what can be done:
1) Lithography: P.R. step coverage problems + stepper DOF limit
2) Stinger after anisotropic etch
3) Metal step coverage problem

Why Isolation? Why LOCOS?

- Need isolation to prevent inversion in the field regions
- LOCOS is used as opposed to other isolations because of its smooth topography

Ideal Goal:

But in reality, topography will greatly limit what can be done:
1) Lithography: P.R. step coverage problems + stepper DOF limit
2) Stinger after anisotropic etch
3) Metal step coverage problem

LOCOS solves all of these problems!
LOCOS introduces several problems of its own:

1) Bird’s beak encroachment into active areas → for 0.5–0.6µm F.O., 0.5µm/side encroachment (thus, 1µm features would disappear!)

2) Excessive redistribution of channel-stop implant

3) Planarity of LOCOS becoming inadequate for submicron needs → Stepper lithography has problems focusing over excessive topography → the smaller the dimensions, the smaller the allowable topography

4) Oxide thickness in closely spaced regions less than in open areas → caused by reduction in oxidants available in narrow openings → minimum spacing allowed: 0.75µm for 5500Å thick oxide

Why the long Bird’s Beak?

The finite pad oxide thickness allows lateral diffusion of reactants → w/o this oxide, there would be no bird’s beak

So why the pad oxide?

→ If deposit nitride directly on Si, get stress cracks in the Si → degrades transistors! → thus, need pad oxide ~200–600Å

As nitride thickness ↑→ stress cracks ↑ → MOS performance ↓
Solution: Reducing the Pad Oxide Thickness

- Local oxidation rate decays exponentially with the distance from the nitride edge.
- The coefficient of the distance is inversely proportional to the square root of pad oxide thickness → reduce pad oxide thickness.

Polybuffered LOCOS

- Polysilicon does not induce as much stress as nitride.
- Use a polysi-oxide layer to buffer against nitride stress.
- Thinner pad oxide → much less lateral diffusion of reactants.
- Result: 0.1-0.2um encroachment for 4000Å F.O. (less than 0.5um with conventional LOCOS).
- Problem: higher step.
Sealed-Interface Local Oxidation (SILO)

**Process Flow:**
1. 100-200Å by thermal nitridation of Si or by CVD → thin nitride layer reduces edge stress and thus # of defects
2. LPCVD SiO$_2$: 250-300Å
3. LPCVD nitride 1500-2000Å
4. Pattern 3-layer masking film via RIE → get some etching of Si*
5. Channel-stop implantation
6. Grow field oxide (F.O.) → get some lateral encroachment of F.O. due to Si etching in 4)

**Result:**
- Very little lateral oxide growth → little LOCOS encroachment: ~0.2µm (caused by overetch into Si at step 4)

**Problem:** get defects if this corner too sharp!

Fully Recessed Oxide LOCOS

**Comments on semi-recessed LOCOS:**
1. Above two processes work due to less lateral oxide growth as pad oxide thickness reduces
2. But both also suffer from steps that are too abrupt → for submicron processes (where steppers are involved in lithography), such steps must be eliminated

**Solution:** Fully Recessed Oxide LOCOS

Create grooves into Si before F.O. oxidation → decreased topography → Less lateral oxide encroachment in some cases
Sidewall-Masked Isolation (SWAMI)

Process Flow:
1) Pad oxide and nitride formation and patterning as in conventional LOCOS and etch grooves into Si (KOH wet etch)*
2) Channel-stop implantation
3) Grow second stress relief oxide (SRO)
4) Deposit second CVD nitride
5) Deposit CVD SiO$_2$
6) Anisotropic etch of HTO/ Si$_3$N$_4$/SiO$_2$
7) Wet etch oxide spacer
8) Grow field oxide (F.O.) → thin nitride sidewall bends up
9) Remove nitride/oxide layers

Result: Very planar isolation w/ excellent topography

Problem:
1) More complex than conventional LOCOS
2) Corner effects: leakage (high ε-field), dislocations, defects…

Tapered Si Sidewall to Reduce Stress

• Use orientation-selective silicon etch, e.g., KOH to achieve ~60° incline when starting wafer is <100> → this reduces stresses when growing F.O. → reduces edge detects

• Edge defects generated at corner points (high stress points)
• High E field at corners for MOS devices → get lower Vth if corner is too sharp → get excessive leakage current

[Teng, IEEE JSSC, 1985]
**Fully Recessed Oxide (FUROX)**

**Process Flow:**
1. Minimum-encroachment LOCOS: using nitrided oxide [(a) & (b)]
   - Nitridation: grow oxide and then 1200°C for 7hrs in NH$_3$
2. Etch away the first F.O. [(c)]
3. Grow 2nd pad oxide 100Å
4. LPCVD nitride 400Å
5. Channel stop implantation [(d)]
6. RIE nitride and 2nd pad oxide [(e)]
7. Grow F.O. [(f)]

**Result:**
- Good planarity, defect(corner)-free, fully recessed oxide
- For 7700Å F.O., Bird’s Beak ~0.15µm

**Problem:**
1. More complex than SWAMI
2. Nitridation generates defects

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**Self-Aligned Planar-Oxidation Technology (SPOT)**

**Process Flow:**
1. Standard LOCOS [(a)]
2. Isotropic oxide etch [(b)]
3. Grow 2nd pad oxide
4. LPCVD 2nd nitride: thinner than 1st [(c)]
5. Anisotropic etch → 2nd nitride shadowed by 1st [(d)]
6. Channel-stop implantation
7. Grow high-pressure F.O.: lower T → less channel-stop implant encroachment [(e)]

**Result:**
- Good planarity

**Problem:**
1. Two F.O. oxidation
2. Still get oxide encroachment!
Process Flow:
1) Standard LOCOS oxide(300Å)/nitride(2400Å) formation and patterning
2) 1st channel-stop implantation
3) 2nd CVD nitride 300Å
4) LPCVD SiO₂: 2000Å
5) RIE 2nd oxide and 2nd nitride (OSELO I)
6) RIE Si ~0.2µm deep (oxide spacer serves as mask)
7) 2nd channel-stop implantation
8) Wet etch oxide spacer
9) Grow F.O. 5500Å

Result:
- 0.8µm isolation length/1.3µm effective isolation length

Problem: RIE Si → sharp corners → defects!

Trench Etch and Refill (Non-LOCOS Isolation)

- Main Applications / 3 Trench Categories
  1) Replacement of LOCOS for isolation of like devices within the same tub in CMOS → Buried oxide (BOX), shallow trench, <1µm
  2) Isolation of n-channel from p-channel devices → preventing latchup in CMOS → moderate depth, 1-3 µm
  3) High packing density trench capacitors in DRAMs → deep trench, >3 µm, <2µm wide
- Main Advantage: no LOCOS-induced Bird’s Beak → higher packing density
Buried-Oxide Isolation (BOX)

Process Flow:
1) Pattern oxide as hard mask
2) Wet etch grooves into Si (KOH) [(a)]
3) Deposit CVD oxide
4) Double-resist process (or, use CMP)
   - Due to “short-range” characteristic of polymer-based planarization →
     good for filling narrow voids with high spatial freq. but not for extensive
     recessed regions
   - 1st P.R. to build up the height of the polymer in recessed regions
   - 2nd P.R. to fill narrow voids
5) Etch back using RIE with same rate for
   P.R. and oxide

Problem: Overetch during etchback → corners → defects, leakage current!
Solution: Add an etch-stop layer → BOX w/ Etch Stop Isolation (BOXES)

Mo serves as etch-stop over Si active areas
Moderate-Depth Trench Isolation

A Latchup-Free CMOS Structure

Process Flow:
1) Grow n-type epitaxial layer
2) Form p-well region
3) Dry etch moderate deep trench at borders of n- and p-regions
4) Refill w/ polysilicon
5) Etch back to give a planar surface

Result:
1) For \( d_{\text{trench}} = 2.5\mu m, w_{\text{trench}} = 1.6\mu m \), need \( d \geq 2\mu m \) (n+ to p+ spacing)
2) For \( d_{\text{trench}} = 2.5\mu m \), need \( d \geq 5.8\mu m \)

Problem: poly trench refill process does not allow trenches of varying widths → only useful for this specific application (i.e., preventing latchup)

Deep, Narrow Trench and Refill

Process Flow:
1) Form/pattern oxide/nitride/oxide hard mask:
2) RIE Si, which requires
   - Smooth tapered sidewalls → void-free refill
   - High Si:mask selectivity and no undercutting of mask
   - Undamaged sidewalls → otherwise will induce leakage
   - Smooth trench bottom → to minimize stress-induced defects that can form after oxide growth
   - Trench depth should be uniform across the wafer and from wafer-to-wafer
3) Grow 500Å oxide, then LPCVD oxide (thick for isolation, thin for capacitors)
4) Refill trench w/ polysilicon
5) Planarize w/ CMP

Result:
1) Very high packing density due to small n+ and p+ separation (can get 1µm-wide trenches), even on standard Si wafers
2) Can eliminate latchup w/ epi on heavily-doped substrate

Problem:
1) Complexity: major problem for isolation, but worth it for DRAMs
2) Only one width allowable for uniform results
Selective Epitaxial Growth (SEG) Isolation

Process Flow:
1) Grow oxide over Si substrate
2) Pattern and RIE oxide down to Si to form active areas
3) Channel-stop implantation
4) Fill trenches using SEG
5) Process CMOS

Result:
1) No bird’s beak
2) F.O. thickness does not depend upon width of the space
3) Planar surface (except for facets)
4) Channel-stop implant removed from S/D regions
5) Can be used for all levels of isolation
6) Can use contacts that fill up the S/D (LOCOS no longer a limitation)

Problem:
1) Facets on the edge of epi → bad topography → solved by CMP
2) sharp corner effects → leakage
3) Leakage due to sidewall inversion → need to increase substrate-doping

Silicon-On-Insulator (SOI) Isolation

Advantages:
1) $C_J$ reduction → faster devices!
2) Much higher density possible → density limited by lithography and etching (not by latchup, oxide encroachment, etc…)
3) Eliminates latchup

Disadvantages:
1) Wafer cost → but always getting cheaper w/ time
2) Poorer Si quality due to manufacture process of SOI wafers (but the quality is getting much better)
   - Process: Implant $O_2^-$ → anneal to form SiO2 → epi to increase usable Si thickness