In this course, the focus will be on silicon microfabrication, but the methods used are also relevant to other material systems, e.g., gallium arsenide, InP, etc.

Materials in Silicon-Based Microfabrication:

- Four basic materials:
  - (a) Silicon (single crystal; polycrystalline)
  - (b) Silicon Dioxide
  - (c) Silicon Nitride
  - (d) Aluminum & Other Metals

- Materials for advanced processes:
  - Tungsten, silicides, polyimide

Need to consider three main items for each material:

- Electrical characteristics
- Chemical characteristics (i.e., stability)
- Usage in IC's

(a) Silicon: (Si)

(i) Single Crystal Silicon (Si)

Electrical: semiconductor
- Can change its conductivity by introducing impurities, called dopants

Semiconductors are not intrinsically conductive
- To make them conductive, replace silicon atoms in the lattice with dopant atoms that have valence bands with fewer or more electrons than the 4 of Si

- If more electrons, then the dopant is a donor: P, As
  - The extra electrons are effectively released from the bonded atoms to join a cloud of free electrons, free to move like electrons in a metal

- If it has fewer electrons than silicon, then the dopant is an acceptor: B
  
  \[
  \text{Si : Si : Si : \text{P} \rightarrow \text{Si : Si : Si : Si : Si : Si}}
  \]

  - Lack of an electron = hole = h^+
  - When electrons move into holes, the holes effectively move in the opposite direction → a h^+ is a mobile (+) charge carrier

Conductivity Equation:

\[
\sigma = q\mu_n n + q\mu_p p
\]

- Nomenclature:
  - \(n^-\) = lightly doped (1014 to 1017)
  - \(n\) = moderately doped (1017 to 1019)
  - \(n^+\) = heavily doped (>1019)

- Chemical: rather inert, but ...
  - can be etched in KOH, HNO3/HF
  - Latter reaction forms oxide first, then etches the oxide with HF

Usage in IC's: active devices (obviously), but also local interconnect, resistors
Silicon Wafer: single-crystal silicon

Silicon crystallography:
- Silicon has a basic diamond structure: two merged face-centered cubic (FCC) crystal structures
- In FCC, atoms are assumed to touch along face diagonals:

Plane nomenclature: Miller indices

- Procedure:
  1. Identify the vector corresponding to the given Miller index.
  2. The plane will be that \( \perp \) to the vector.

Miller Indices \((h k l)\):
- Planes
  - Reciprocal of plane intercepts with axes
  - e.g., for \((110)\), intersects \(x,y,z\) = \((1,1,0)\); reciprocals: \((1,1,0) \rightarrow (110)\)
  - (unique), \(\{111\}\)
- Directions
  - One endpoint of vector @ origin
  - \(\{111\}\), \(\{110\}\)
- The angle between vectors \([abc]\) and \([xyz]\) is given by:
  \[
  \theta_{[a,b,c]}(x,y,z) = \cos^{-1} \left( \frac{ax + by + cz}{(a,b,c) \cdot (x,y,z)} \right)
  \]
- For \((100)\) and \((110)\) \(= 45^\circ\)
- For \((100)\) and \((111)\) \(= 54.74^\circ\)
- For \((110)\) and \((111)\) \(= 35.26^\circ, 90^\circ, \) and \(144.74^\circ\)

- Planes on a silicon wafer:
  - Very pure: 1 in \(10^{10}\) impurity level
Very low defect density: 1-3/cm²
Different sizes over the years:
- 1974: 2" (50mm)
- 1979: 3" (75mm)
- 1984: 4" (100mm)
- 1986: 5" (125mm)
- 1990: 6" (150mm)
- 1997: 8" (200mm)
- 2001: 12" (300mm)
- 2012: 17" (450mm)

Why go to larger wafers?
1. Quality goes up (will explain later)
2. Yield gets better (reduces cost/chip)
   \[ \text{No. of chips per wafer} \sim \frac{D^2}{2} \]
   \[ \text{Productivity cost/wafer} \sim D^{n} \]

<table>
<thead>
<tr>
<th>Wafer Size</th>
<th>Damage Factor</th>
<th>No. Chips</th>
<th>Cost/Wafer</th>
<th>Cost/Chip</th>
</tr>
</thead>
<tbody>
<tr>
<td>4&quot;</td>
<td>1</td>
<td>N</td>
<td>C</td>
<td>C/N</td>
</tr>
<tr>
<td>6&quot;</td>
<td>1.5</td>
<td>2.25N</td>
<td>1.5C</td>
<td>0.67(C/N)</td>
</tr>
</tbody>
</table>

Of course, the cleanliness of the clean room also greatly influences the yield
- Class 100: no more than 100 particles larger than 0.5 μm in one cubic meter
- In addition, you can get more chips on a larger wafer, since you waste less space along the edges

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Doping concentration/resistivity
- Type: either p or n
- Concentration: $10^{13} - 10^{20}$ cm$^{-3}$

Polycrystalline silicon (polySi)
- Basically, grains of silicon
- Electrical:
  - Result: conducts when doped, like single crystal silicon, but now has grain boundaries that impede

- Wafer orientation:
  - $\langle 100 \rangle$ used in CMOS
  - $\langle 111 \rangle$ used for bipolar transistors
  - Higher surface mobility
  - Fewer Si-Si dangling bonds
  - Less interface charge
  - In CMOS, the e-h travel along the surface (inversion layer)

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conduction at low to moderate doping levels (and increase conduction at extremely high degenerate doping levels)
  - Chemical: same as single crystal silicon
  - Usage in IC’s: gate material in MOSFET’s, local interconnect

- Also used quite heavily in MEMS as a structural material

- Deposition:
  - Most common technique: chemical vapor deposition (CVD)

  ⇒ done in a furnace: (low pressure CVD → LPCVD)

  ⇒ heating filament → maintain temperature
  585°C → 610°C and 610°C

  ⇒ Silane (SiH₄) + low pressure + heat reactor

  ⇒ exhaust (reaction by-products)

  ⇒ deposited polysilicon

- Grain size → strong function of temperature
  - Depends on the ability of adatoms to run around and find the lowest energy state locations → leads to large grain size
  - At 610°C, grain size is 200nm or so
  - At 585°C, the Si comes down amorphous, but then can be crystallized into very fine grains by annealing

- Doping concentration/resistivity:

  ![Graph showing resistivity vs. doping concentration](image)

  - This almost binary resistance dependence on doping is fairly unique to polysilicon ... and quite useful ... why does it happen?
    - If you apply an E-field, then
      → If low doping, e⁻’s can’t get by the grain boundaries: they get trapped in the traps
      → If high doping, e⁻’s can now get by the grain boundaries

(b) Silicon Dioxide (SiO₂):
  - Amorphous structure (this is NOT quartz)
  - Electrical: insulator

  ![Graph showing probability of hopping](image)

  - Resistivity: 10¹⁵ – 10¹⁸ Ω·cm
    - Compare to Al’s 10⁻⁵ Ω·cm
  - Chemical: fairly inert, but etches in HF
  - Usage in IC’s: gate dielectric in MOSFET, sacrificial layer in MEMS

(c) Silicon Nitride (Si₃N₄)
  - Electrical: insulator

  ![Graph showing energy levels](image)

  - Can be deposited or grown thermally

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(c) Silicon Nitride (Si₃N₄)
  - Electrical: insulator

  ![Graph showing energy levels](image)
- Chemical: fairly inert, but etches in hot phosphoric acid
- Usage in IC's: insulator, as in metal-to-metal insulation in MOSFET's and interconnect insulation in MEMS
- Usually deposited via chemical vapor deposition (CVD)
  - Reactants: SiH₄ + NH₃

(d) Aluminum: (Al)
- Electrical: conductor; 20x10⁻⁶ Ω·cm
- Chemical: active; can be etched in many acids
- Usage in IC's: interconnect; gate material (metal gate technology before 1974, and after 2007)
- Deposited via thermal evaporation, e-beam evaporation, or sputtering
  - Melting point: ~550°C
- Structure:
  - In IC's, the polycrystalline form is normally seen, with grains on the order of 100nm

- Why is Al preferred among many other metals?
  - What do we want in a metal?
    → It must conduct.
    → It must stick to SiO₂.
  - Al does both of these
  - Au, Ag, and other metals can be used, but they require a layer between them and the SiO₂ to help them stick (need an adhesion layer)