EE 143: Microfabrication Materials 9/4/14Th

- Reading: portions throughout Jaeger
- Lecture Topics:
  - Silicon
  - Silicon Dioxide
  - Silicon Nitride
  - Aluminum & Other Metals
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- In this course, the focus will be on silicon microfabrication, but the methods used are also relevant to other material systems, e.g., gallium arsenide, InP, etc.
- Materials in Silicon-Based Microfabrication:
- Four basic materials
  (a) Silicon (single crystal; polycrystalline)
  (b) Silicon Dioxide
  (c) Silicon Nitride
  (d) Aluminum & Other Metals
- Materials for advanced processes
  - Tungsten, silicides, polyimide
- Need to consider three main items for each material
  - Electrical characteristics
  - Chemical characteristics (i.e., stability)
  - Usage in IC's
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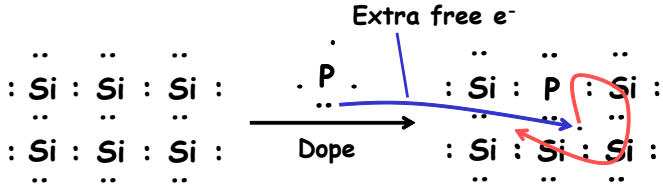
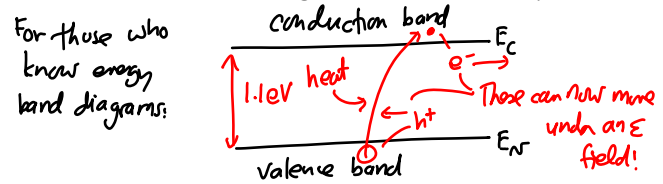
(a) Silicon: (Si)
(i) Single Crystal Silicon (Si)

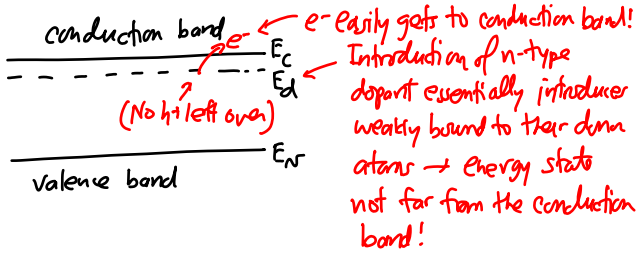
- Electrical: semiconductor
  - Can change its conductivity by introducing impurities, called dopants
- Semiconductors are not intrinsically conductive
- To make them conductive, replace silicon atoms in the lattice with dopant atoms that have valence bands with fewer or more e⁻'s than the 4 of Si
- If more e⁻'s, then the dopant is a donor: P, As
  - The extra e⁻ is effectively released from the bonded atoms to join a cloud of free e⁻'s, free to move like e⁻'s in a metal



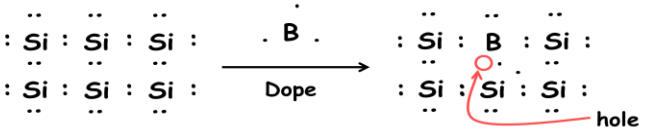
  - The larger the # of donor atoms, the larger the # of free e⁻'s → the higher the conductivity



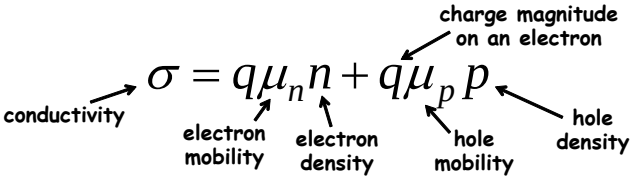
- Here, energy (e.g., heat that raises temperature) can give an e⁻ in the valence band sufficient energy to get to the conduction band
- This puts an e⁻ in the conduction band and a h⁺ in the valence band, both of which can conduct
- Doping basically adds an atom with one e⁻ that is only loosely held to the atom; so very little energy (e.g., from an electric field) is needed to strip it from the atom and let it wander the conduction band



- If it has fewer e⁻'s than silicon, then the dopant is an acceptor: B

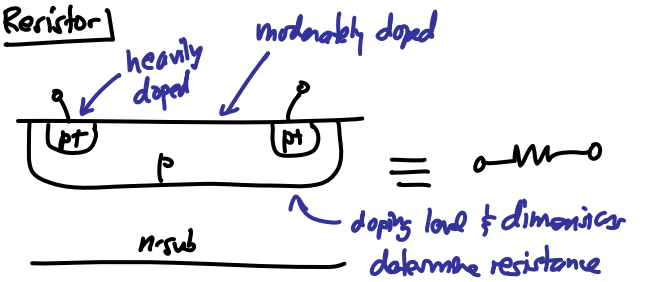


  - Lack of an e⁻ = hole = h⁺
  - When e⁻'s move into h⁺'s, the h⁺'s effectively move in the opposite direction → a h⁺ is a mobile (+) charge carrier
- Conductivity Equation:

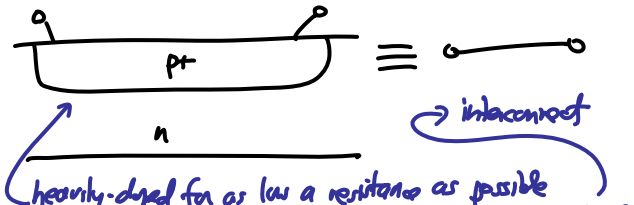


- Nomenclature:
  - n- = lightly doped (1014 to 1017)
  - n = moderately doped (1017 to 1019)
  - n+ = heavily doped (>1019)
- Chemical: rather inert, but …
- can be etched in KOH, HNO3/HF
- Latter reaction forms oxide first, then etches the oxide with HF
- Usage in IC's: active devices (obviously), but also local interconnect, resistors

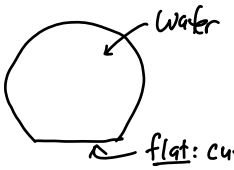
Resistor



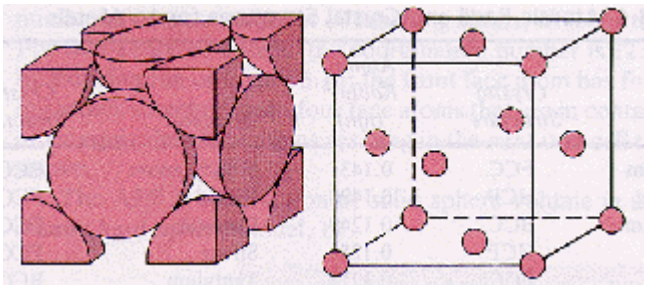
Interconnect (basically want this to behave like a metal)

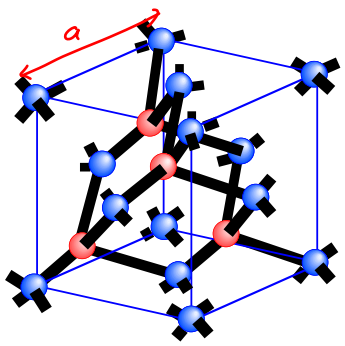


- Silicon Wafer: single-crystal silicon



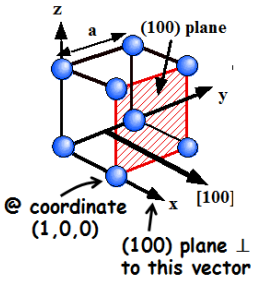
- Silicon crystallography:
  - Silicon has a basic diamond structure: two merged face-centered cubic (FCC) crystal structures
  - In FCC, atoms are assumed to touch along face diagonals:



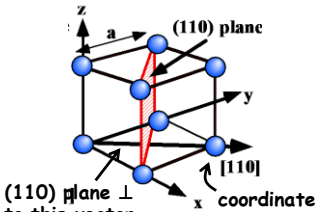


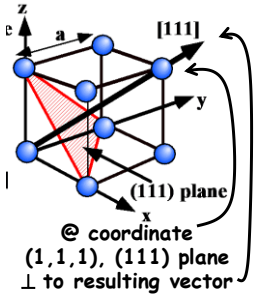
Two merged FCC cells offset by $(\frac{a}{4})$ in the x, y, and z axes.

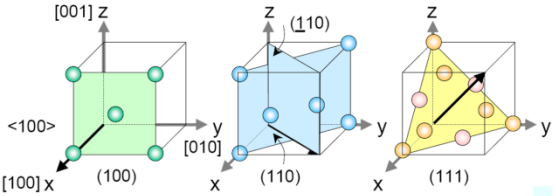
- Plane nomenclature: Miller indices



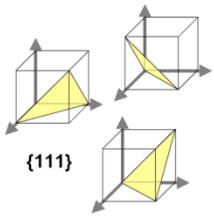
⇒ Procedure:
① Identify the vectors corresponding to the given Miller indices.
② The plane will be that ⊥ to the vectors.







Miller Indices (h k l):
- Planes
  - Reciprocal of plane intercepts with axes
  - e.g., for (110), intercepts: (x,y,z) = (1,1,∞); reciprocals: (1,1,0) → (110)
  - (unique), {family}
- Directions
  - One endpoint of vector @ origin
  - [unique], <family>



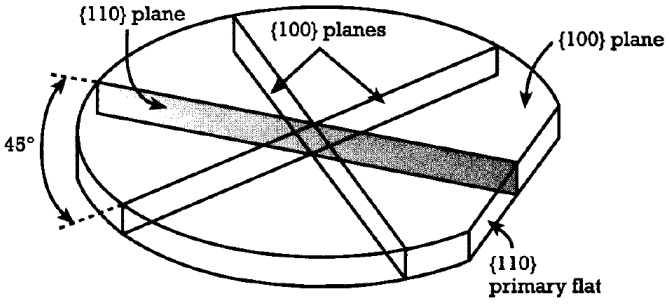
- The angle between vectors [abc] and [xyz] is given by:

$$ax + by + cz = |(a,b,c)| \cdot |(x,y,z)| \cdot \cos\theta$$

$$\theta_{(a,b,c),(x,y,z)} = \cos^{-1}\left[\frac{ax+by+cz}{|(a,b,c)| \cdot |(x,y,z)|}\right]$$

- For {100} and {110} → 45°
- For {100} and {111} → 54.74°
- For {110} and {111} → 35.26°, 90°, and 144.74°

- Planes on a silicon wafer:



{100} type wafer

  - Very pure: 1 in 10^{10} impurity level

- Very low defect density: 1-3/cm^2
- Different sizes over the years:
  - → 1974: 2" (50mm)
  - → 1979: 3" (75mm)
  - → 1984: 4" (100mm)
  - → 1986: 5" (125mm)
  - → 1990: 6" (150mm)
  - → 1997: 8" (200mm)
  - → 2001: 12" (300mm)
  - → 2012: 17" (450mm)

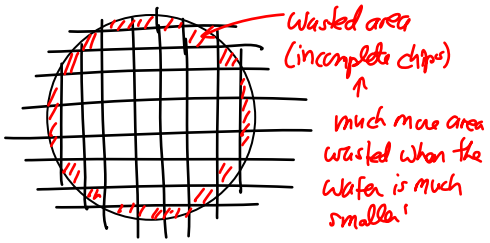
- Why go to larger wafers?
  1. Quality goes up (will explain later)
  2. Yield gets better (reduces cost/chip)

No. of chips per wafer ~ D^2 (↑ diameter of wafer)

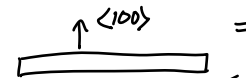
Production cost/wafer ~ D^n (↑, $1 < n < 2$)

Wafer Size	Diameter Scale Factor	No. Chips	Cost/ Wafer	Cost/ Chip
4"	1	N	C	C/N
6"	1.5	2.25N	1.5C (↑ for n=1)	0.67(C/N) (↑ Cheaper!)

- Of course, the cleanliness of the clean room also greatly influences the yield
  - Class 100: no more than 100 particles larger than 0.5 μm in one cubic meter
- In addition, you can get more chips on a larger wafer, since you waste less space along the edges

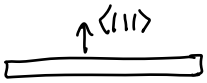


- Wafer orientation:



⇒ used in CMOS
① higher surface mobility
② fewer Si-SiO$_2$ dangling bonds
∴ less interface charge

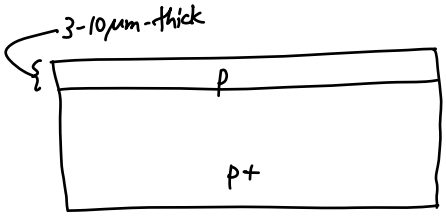
in MOS, the e- & ht travel along the surface (the inversion layer)



⇒ used for bipolar transistors (get least pattern shift)

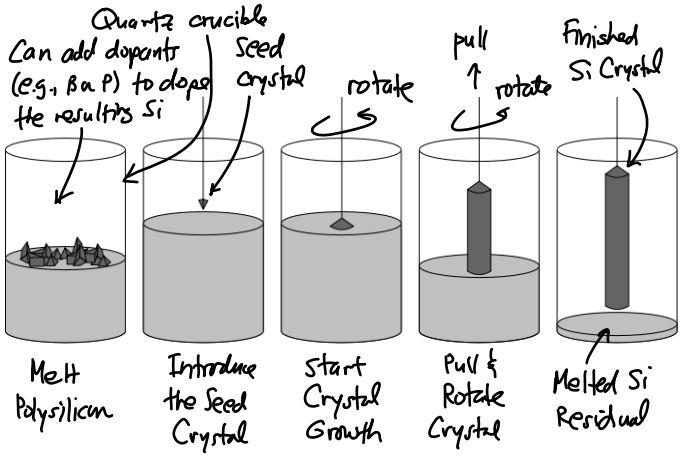
- Doping concentration/resistivity
  - Type: either p or n
  - Concentration: 10^{13} - 10^{20} cm^{-3}

Common Starting CMOS Wafer (p on p+ wafer)



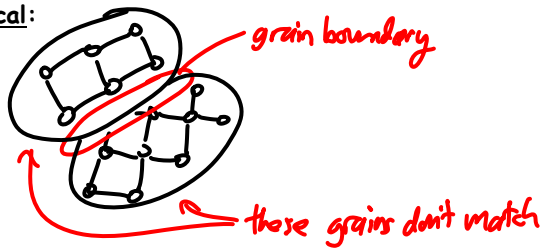
⇒ we'll see that this provides better latchup immunity

- Flatness:
  - Very important for lithography, where focusing is needed
  - For 8" wafer, flatness must be better than ±200nm
  - Polishing technology critical for wafer production
- Wafer production:
- Generally use the Czochralski method, invented by Jan Czochralski in 1916 while investigating the crystallization rates of metals
- Finished crystal can be up to 2 meters long
- Must control temperature and velocity fields during crystal growth to minimize defects



(ii) Polycrystalline silicon (polySi)

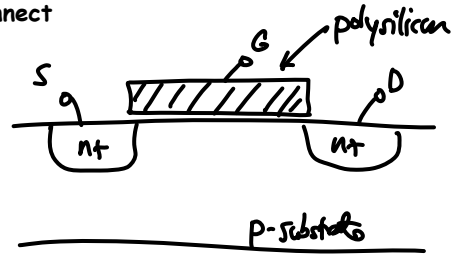
- Basically, grains of silicon
- Electrical:



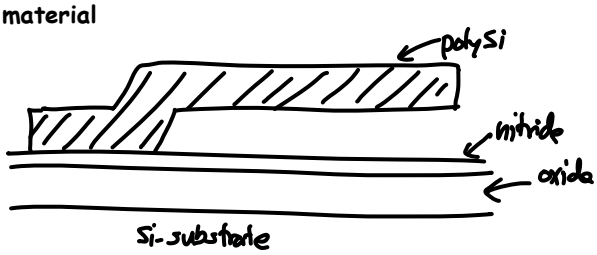
- Result: conducts when doped, like single crystal silicon, but now has grain boundaries that impede

conduction at low to moderate doping levels (and increase conduction at extremely high degenerate doping levels)

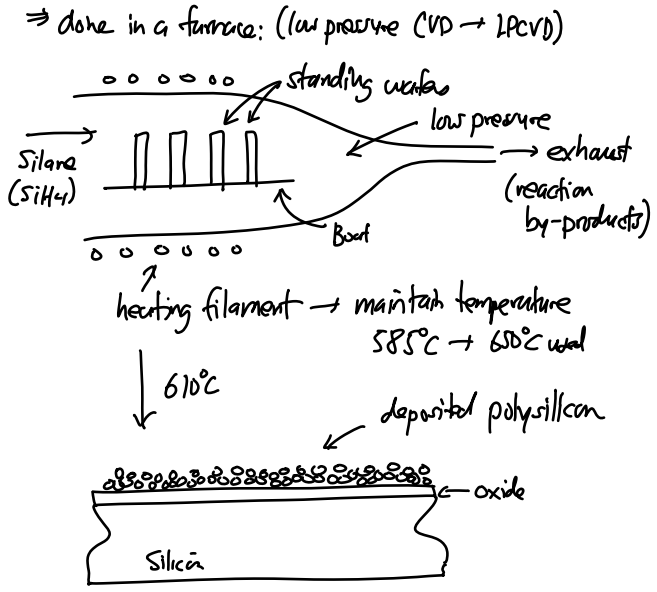
- Chemical: same as single crystal silicon
- Usage in IC's: gate material in MOSFET's, local interconnect



  - Also used quite heavily in MEMS as a structural material

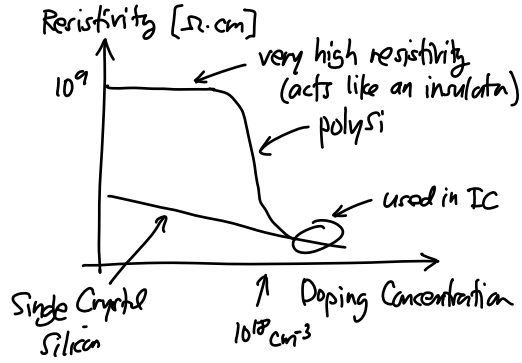


- Deposition:
  - Most common technique: chemical vapor deposition (CVD)



- Grain size → strong function of temperature
  - Depends on the ability of adatoms to run around and find the lowest energy state locations → leads to large grain size
  - At 610°C, grain size is 200nm or so
  - At 585°C, the Si comes down amorphous, but then can be crystallized into very fine grains by annealing

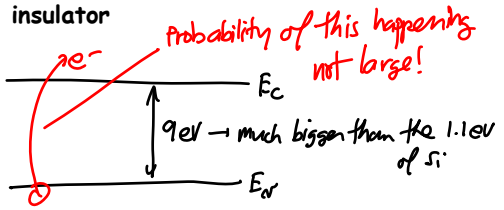
- Doping concentration/resistivity:



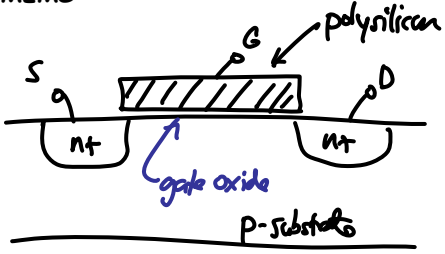
- This almost binary resistance dependence on doping is fairly unique to polysilicon … and quite useful … why does it happen?
  - If you apply an E-field, then
    - → If low doping, e⁻'s can't get b the grain boundaries; they get trapped in the traps
    - → If high doping, e⁻'s can now get by the grain boundaries
- ----------

(b) Silicon Dioxide (SiO_2):

- Amorphous structure (this is NOT quartz)
- Electrical: insulator



- Resistivity: 10^{14} – 10^{18} Ω·cm
  - Compare to Al's 10^{-5} Ω·cm
- Chemical: fairly inert, but etches in HF
- Usage in IC's: gate dielectric in MOSFET, sacrificial layer in MEMS



- Can be deposited or grown thermally
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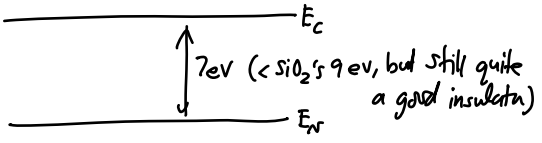
(c) Silicon Nitride (Si_3N_4)

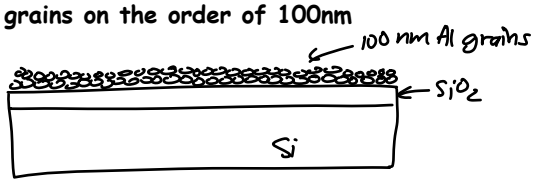
- Electrical: insulator



- Chemical: fairly inert, but etches in hot phosphoric acid
- Usage in IC's: insulator, as in metal-to-metal insulation in MOSFET's and interconnect insulation in MEMS
- Usually deposited via chemical vapor deposition (CVD)
  - Reactants: SiH_4 + NH_3
- ----------

(d) Aluminum: (Al)

- Electrical: conductor; $20 \times 10^{-6}\ \Omega \cdot cm$
- Chemical: active; can be etched in many acids
- Usage in IC's: interconnect; gate material (metal gate technology before 1974, and after 2007)
- Deposited via thermal evaporation, e-beam evaporation, or sputtering
  - Melting point: ~550°C
- Structure:
  - In IC's, the polycrystalline form is normally seen, with grains on the order of 100nm



- Why is Al preferred among many other metals?
  - What do we want in a metal?
    - → It must conduct.
    - → It must stick to SiO_2.
  - Al does both of these
  - Au, Ag, and other metals can be used, but they require a layer between them and the SiO_2 to help them stick (need an adhesion layer)
- ----------