Lecture 5: Process Module Overview II

- Announcements:
  - ↳ Lab sections now settled
  - ↳ HW#2 online
  - ↳ Moving my Monday office hour to 1:30 p.m.
  - ↳ Moving lecture to 180 Tan Hall (from now on)
- ------------------------------------
- Lecture Topics:
  - ↳ Process Modules (review & cont.)
  - ↳ Photolithography, Etching, Oxidation, Film Deposition, Ion Implantation, Diffusion
  - ↳ Process Integration (Example NMOS Process)
- ------------------------------------

Process Modules

⇒ there are actually only a few basic modules used for processing

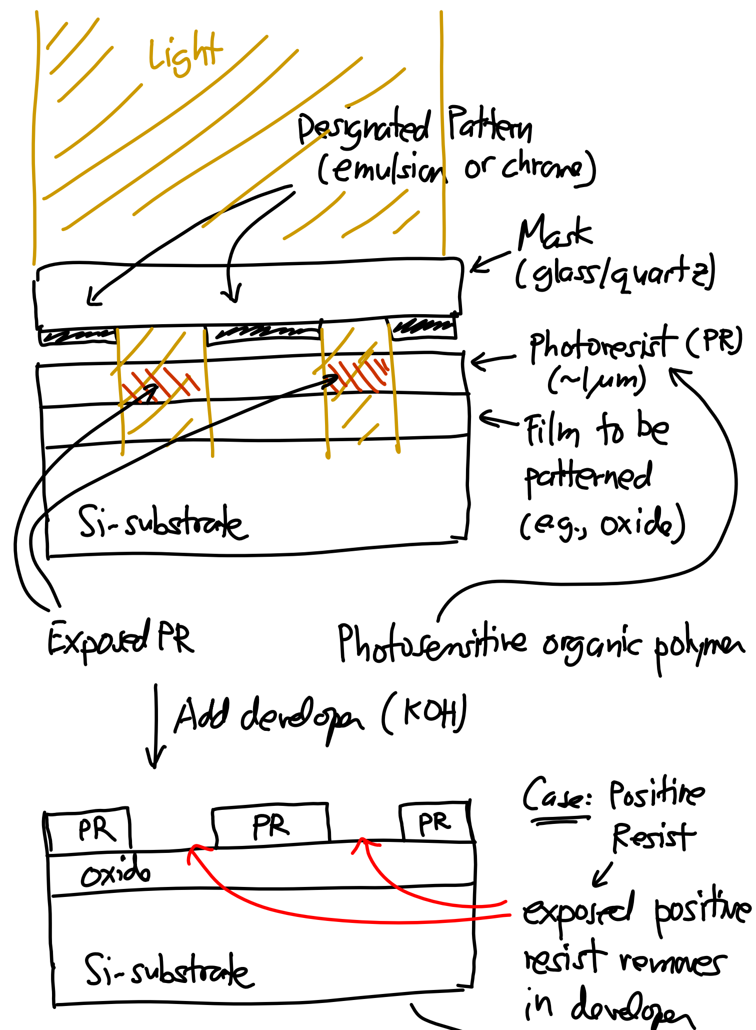
↓

Combination of these in the correct sequence yields an integrated circuit technology that provides transistors, MEMS, nanodevices, etc.

⇒ For each module, need to understand:

1. Physics and engineering of each module in detail.
2. Interactions between modules.
3. The effect of each module on the finished device.

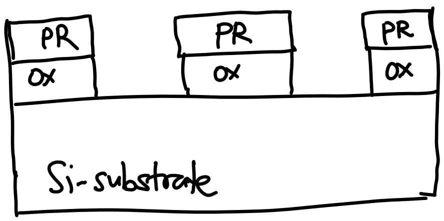
Photolithography



⇒ Now, the PR is patterned
⇒ Ready for the next step: Etching

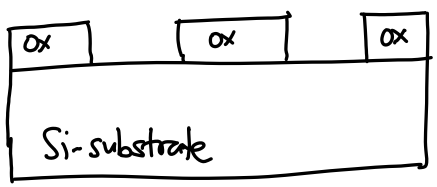
↓ *

↓ Etch oxide (using dry or wet etchant)



⇒ PR protects underlying oxide from etching

↓ Acetone or PRS3000 (to remove the PR)



} oxide film now patterned

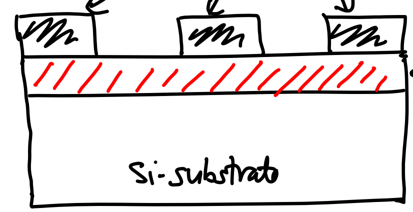
⇒ Above: collectively called a masking step

Number of Masking Steps

- NMOS: 4-6 masks
- 1990 CMOS: 8–11 masks
- today's CMOS: >28 masks
- Bipolar: 11–13 masks
- BiCMOS: 20 masks
  - combination of bipolar & CMOS (mainly for RF/wireless apps.)

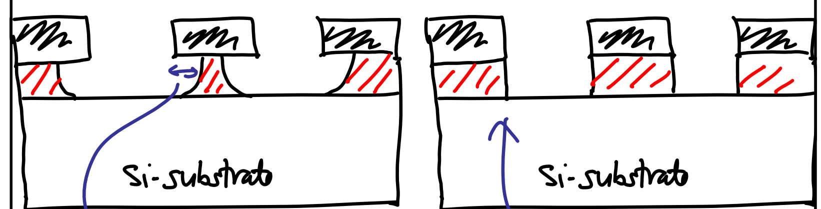
Usually gauge the cost & complexity of a given technology by the # masking steps!

Etching



{ Etches the same rate in all directions } Isotropic Etch

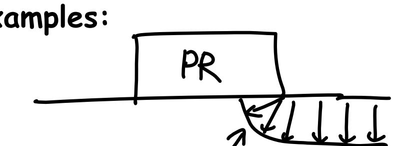
Anisotropic Etch { Etches in only one direction (e.g., straight down)



undercutting
↳ not desirable when resolution is important
↳ very desirable in MEMS, when a structure must be released

no undercutting
↳ best resolution!

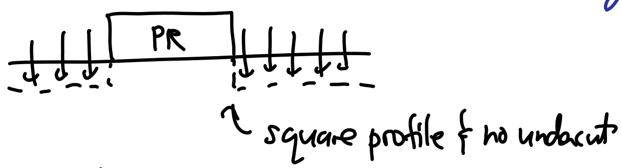
- Isotropic Etchant Examples:
  - Wet etchants
  - Dry plasma etch



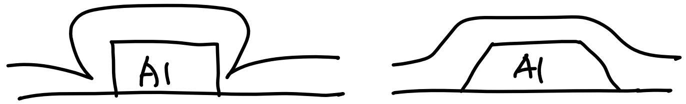
get undercut & curved profile

- Anistropic Etchant Examples:
  - Reactive ion etch
  - Ion milling

  } Use ions under E-fields to give the etch more directionality.



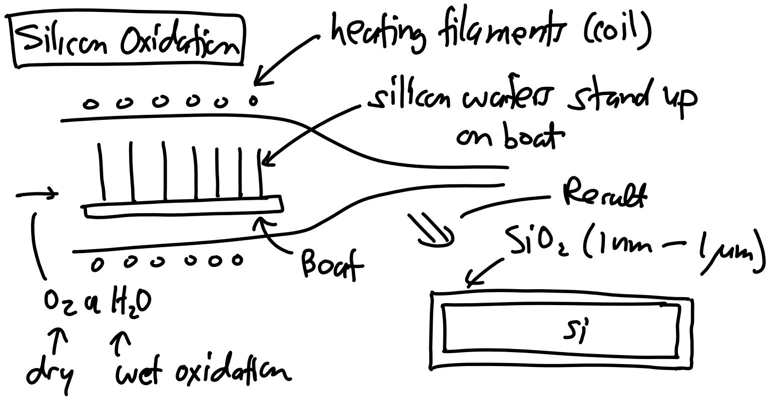
- Remarks:
  - Wet etching is fairly cheap
  - Dry etching requires a plasma, so requires some expensive equipment
  - Don't always want straight sidewalls



Too much topography → more difficult for subsequent films to conform

Sloped sidewalls allow better conformability

Silicon Oxidation

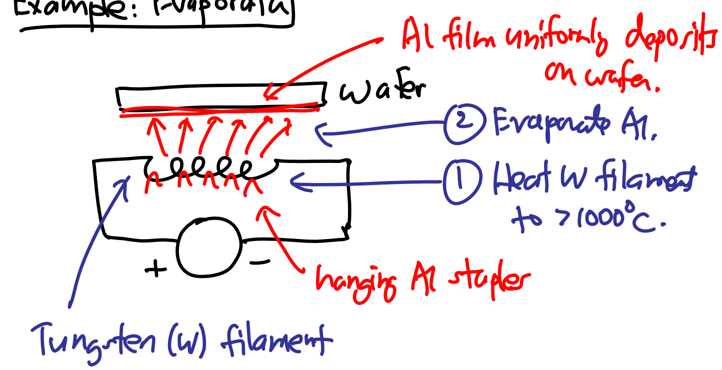


- Remarks:
  - Uniformity can be better than 2% across the wafer from lot to lot
  - Need to flow the O_2 fairly fast in order to minimize reactant losses from the first boat to the last one

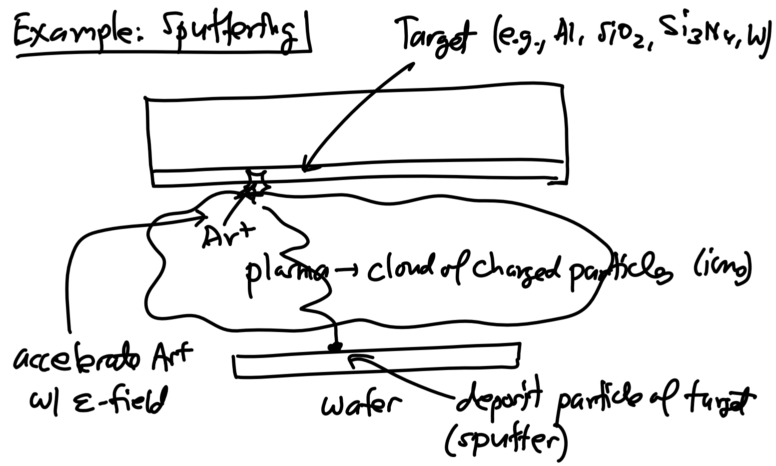
Thin-Film Deposition:

- For deposition of films like Al (and other metals), SiO_2, Si_3N_4, and polysilicon
- Deposition, not thermal growth

Example: Evaporation

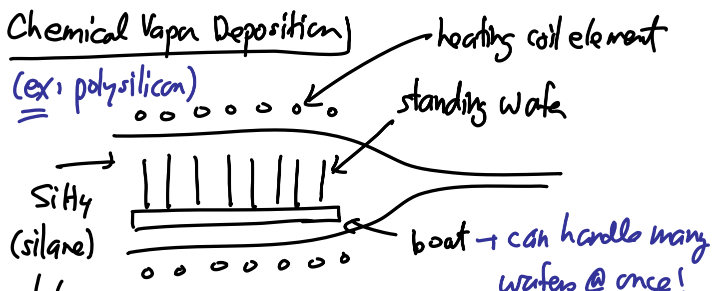


Example: Sputtering



- Also, have chemical vapor deposition (CVD)
  - Chemical reaction involved in deposition of a given thin film
  - High temperature, but not nearly as high as often required for thermal growth

Chemical Vapor Deposition
(ex: polysilicon)

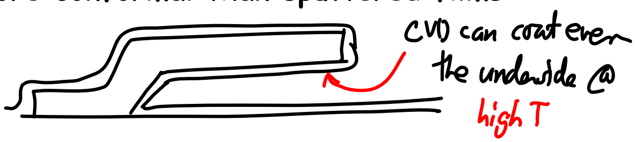


585°C – 600°C for polysilicon
chemically decomposes to deposit poly Si

$$SiH_4 \xrightarrow{600^\circ C,\ 25\text{–}150\,Pa} Si + 2H_2$$

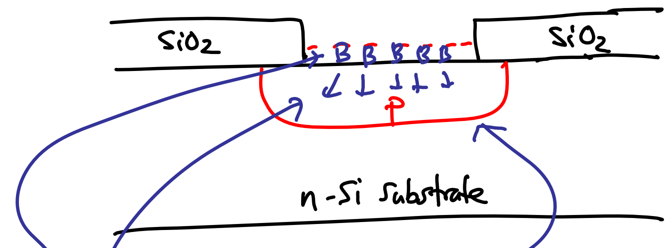
600°C ← fairly high T
25–150 Pa ← low pressure (LPCVD)

- **Remarks**:
  - Lot's of materials can be deposited in a similar manner: polysilicon, SiO_2, Si_3N_4, tungsten
  - Compared to sputtering, CVD is less expensive since one can coat many wafers at once; sputtering generally does it one at a time
  - For higher temperature, CVD films are much more conformal than sputtered films



- **Diffusion**:
- Process of introducing dopants into selected areas on an IC
- **Example**:

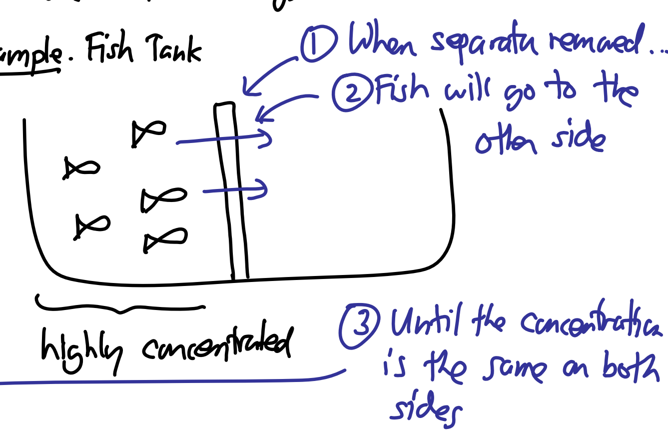
diborane gas → $B_2H_6 + O_2$ @ high temperature ~800°C – 1200°C



① Form borosilicate glass w/ high B concentration
② Boron diffuses in → this becomes p-type

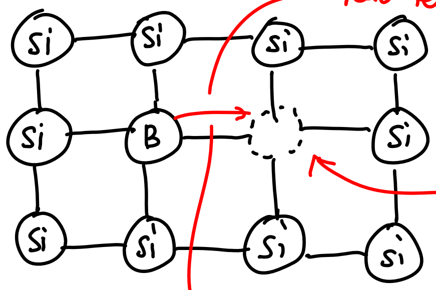
⇒ diffusion requires:
① concentration gradient
② movement (velocity)

→ Example: Fish Tank



But they can't if they're dead!

It's similar for an impurity in silicon:



need temperature for this to happen

Need higher T for this vacancy to exist.

Just one mechanism for diffusion → we'll look at others, too

Substitutional diffusion:
⇒ impurity moves along vacancies in the lattice
⇒ substitutes for a Si atom in the lattice

For movement to occur:

1. Vacancies must exist.
2. The B must have enough energy to move.

Both require high temperature!

must heat to induce diffusion of impurities in Si!

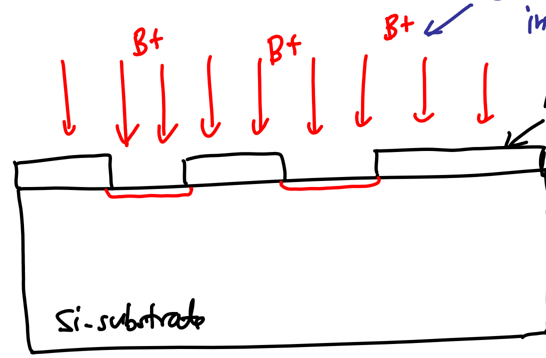
Definitions:

1. **Predeposition**: diffusion w/ dopant source present
2. **Drive-in**: diffusion in an inert ambient, e.g., N_2 w/ no dopant gases present

Ion Implantation

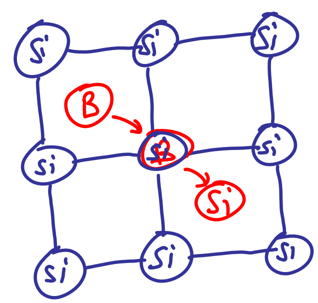
⇒ a more accurate way to introduce dopants before drive-in

① Accelerate B^+ ions into the Si-substrate



Masking layer (e.g., oxide or PR)

② B+ punches into the Si



③ Raise T to move the B into the lattice → only when it's in the lattice is it active & can contribute to the doping level

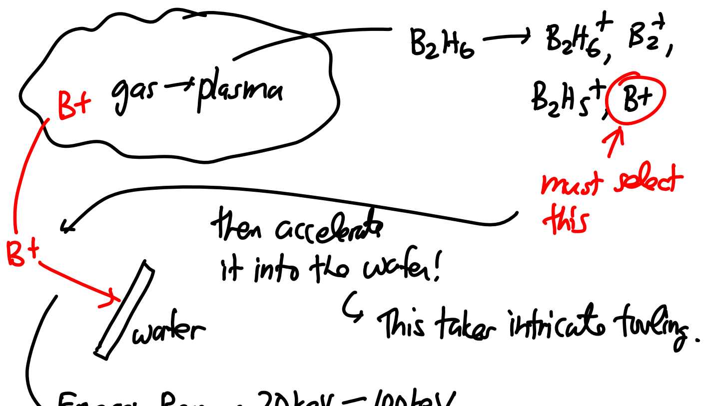
④ Keep T up to drive the dopants in to the desired depth.

Advantages:

1. accurate dose
2. change depth by setting ion energy
3. no need for high temperature

Problem: COST!

An ion implanter is quite a sophisticated piece of equipment! → and expensive! (> $1 million)



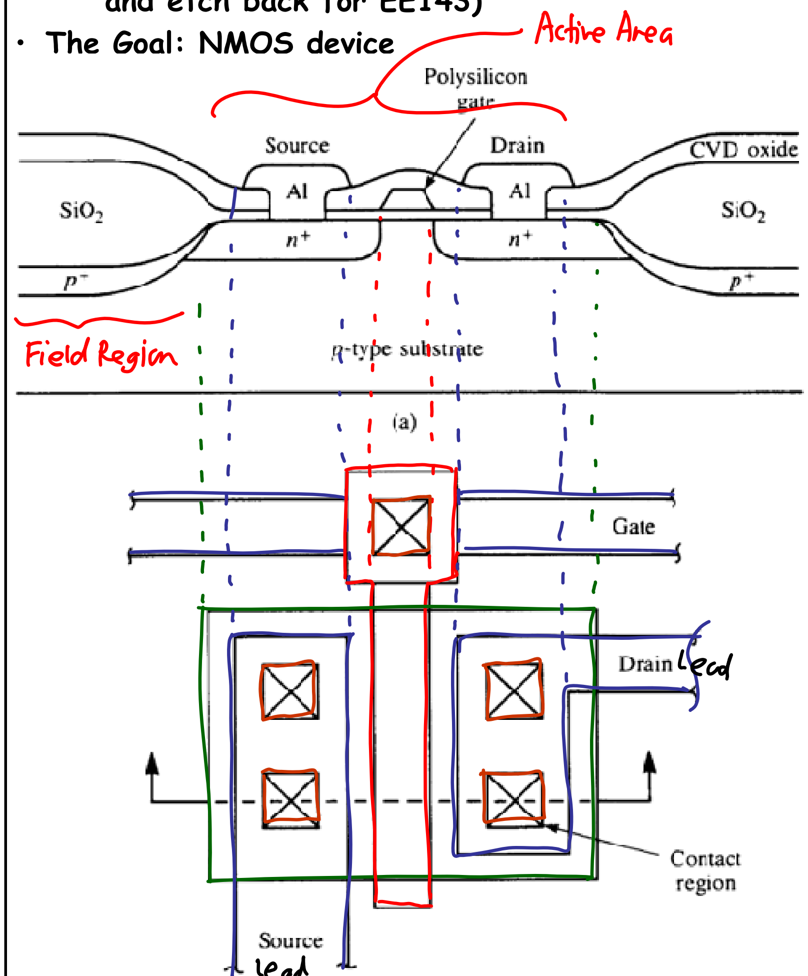
Energy Range: 20keV – 100keV

Penetration Depth: fraction of a μm

⇒ larger ions don't go as far as smaller (heavier ions penetrate shallower than smaller)

Dose: $10^{11} - 10^{15}\ cm^{-2}$

- **Process Integration**:
- e.g., Standard NMOS Process
- Similar to EE143 process, but a bit more advanced
- Difference:
  - ↳ 5 masks (vs. 4 for EE143)
  - ↳ LOCOS oxidation (local oxidation) (oxidation and etch back for EE143)
- The Goal: NMOS device



5 Masks

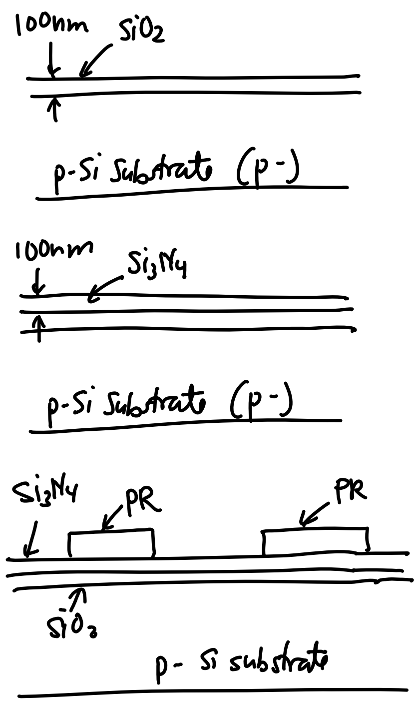
- Gate Polysilicon Mask (cf)
- Active Area Mask (cf)
- Contact Mask (df)
- Metal Mask (cf)
- Bond Pad Opening Mask (df) → not shown

clear field → for (+) PR box indicates regions of PR that remain after lithography

dark field → for (+) PR box indicates region of PR removed after lithography

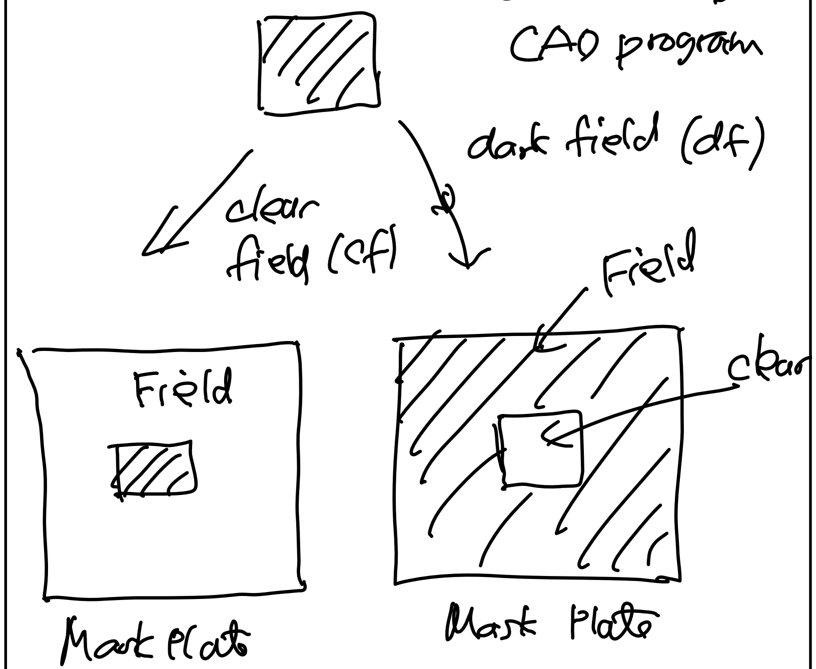
NMOS Process Flow

Silicon Oxidation thickness = 100nm
↓
LPCVD Si_3N_4 (100nm)
↓
Mask I: Active Region
↓
over →

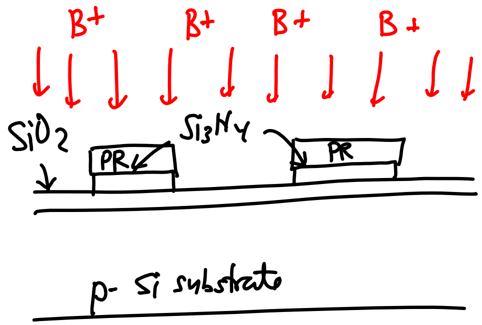


Dark Field vs. Clear Field Masks

Layout → on a computer screen using a CAD program

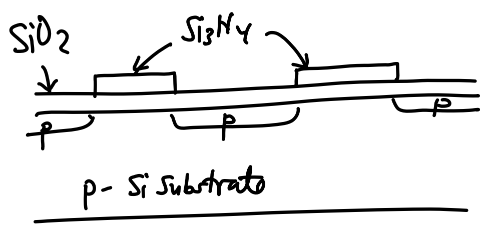


Etch 100nm of Si_3N_4



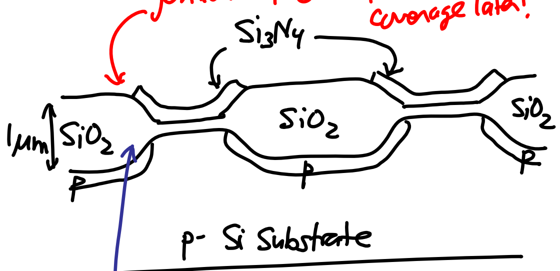
Field Isolation Implant: p-type

Remove PR

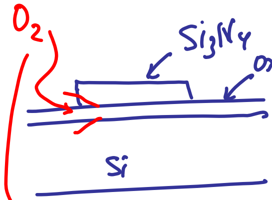


Thermal Oxidation of Si (1μm LOCOS)

gentler topography for better coverage later!

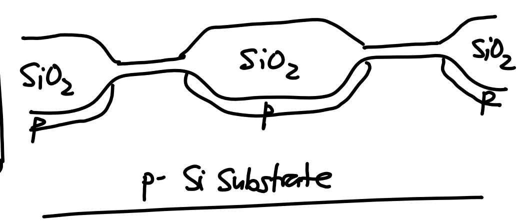


Bird's beak region
↳ why do we get this?

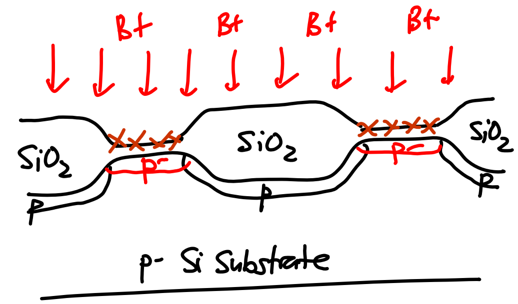


Reactants get under the nitride @ edges → oxide grows
& bends the Si_3N_4

Etch All Si_3N_4 (blanket wet etch; no mask)



Threshold Voltage Implant: B+ (no mask)

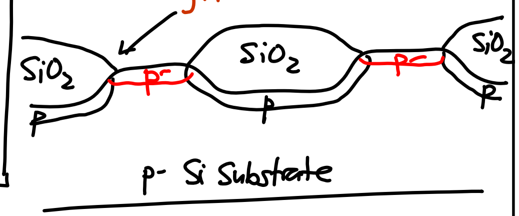


LOCOS oxidation serves as mask
↳ implant only gets into active areas (where it should be)

⇒ Now, the oxide above the active area is damaged → can't use it as the gate oxide, since the gate oxide must be pure & defect free! → must regrow it!

Remove 100nm of Damaged Oxide (wet etch → hydrofluoric acid (HF))

gate oxide removed



EE 143: Microfabrication Technology
Lecture 5w: Process Modules II

CTN 9/11/14