EE143 – Fall 2016
Microfabrication Technologies

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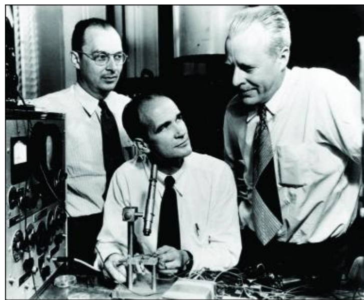
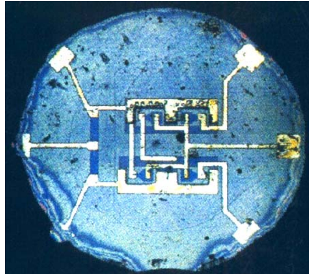
Invention of Transistors - 1947

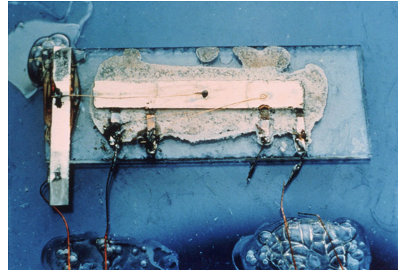


Bardeen, Shockley, and Brattain at Bell Labs - Brattain and Bardeen invented the bipolar transistor in 1947.

Point contact Ge bipolar transistor

The First Integrated Circuits - 1958





R. N. Noyce
Fairchild Semiconductor
Co-Founder of both
Fairchild and Intel
(deceased 1990)

"Unitary Circuit" made of Si

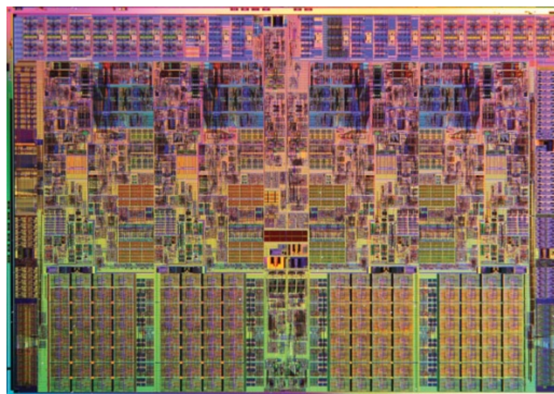
Jack Kilby
Texas Instruments
Invented IC during his first year at TI

(Nobel Prize 2000)

"Solid Circuit" made of Ge

Intel Core i7 Microprocessor (4 Cores)

~ 1.1 Billion Transistors



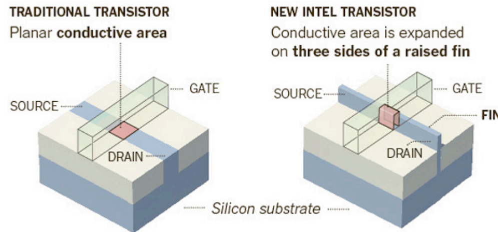
Most powerful processor has about 10B transistors today.
Most powerful FPGA has 20B+ transistors.
http://en.wikipedia.org/wiki/Transistor_count

New Transistor Grows in the Third Dimension

The new Intel transistor provides higher performance by increasing the conductive area between the source and drain regions of the chip, allowing more current to flow through.

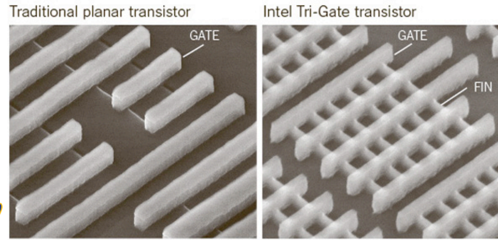
TRADITIONAL TRANSISTOR
Planar **conductive area**

NEW INTEL TRANSISTOR
Conductive area is expanded on **three sides of a raised fin**



The new transistor with its raised **fin** requires a smaller footprint, allowing more of them to fit in a computer chip. The new design can also reduce power consumption, yielding better battery life on devices.

Traditional planar transistor | Intel Tri-Gate transistor



Source: Intel

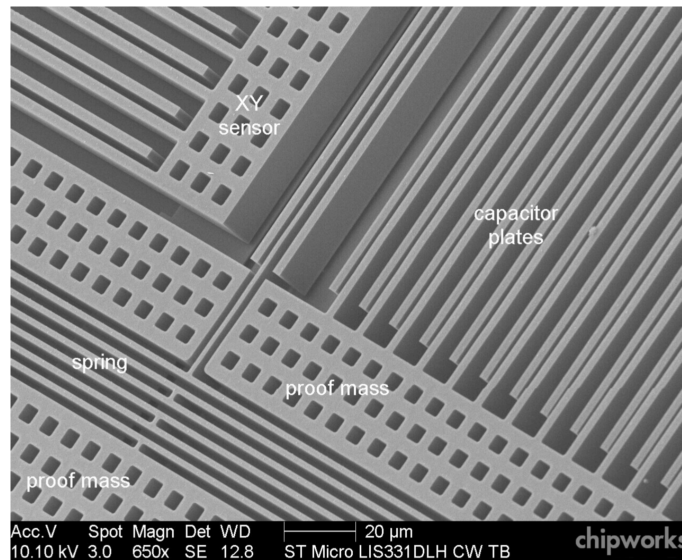
THE NEW YORK TIMES

FinFET

- **Invented at Berkeley !**
- Hisamoto, D.; Wen-Chin Lee; Kedzierski, J.; Takeuchi, H.; Asano, K.; Kuo, C.; Anderson, Erik; Tsu-Jae King; Bokor, J.; Chenming Hu, "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Transactions on Electron Devices,* 2000

http://www.nytimes.com/imagepages/2011/05/05/science/05chip_graphic.html?action=click&contentCollection=Science&module=RelatedCoverage®ion=Marginalia&pgtype=article

MEMS Sensors (Inertia Sensors)



www.memsjournal.com/2010/12/motion-sensing-in-the-iphone-4-mems-accelerometer.html

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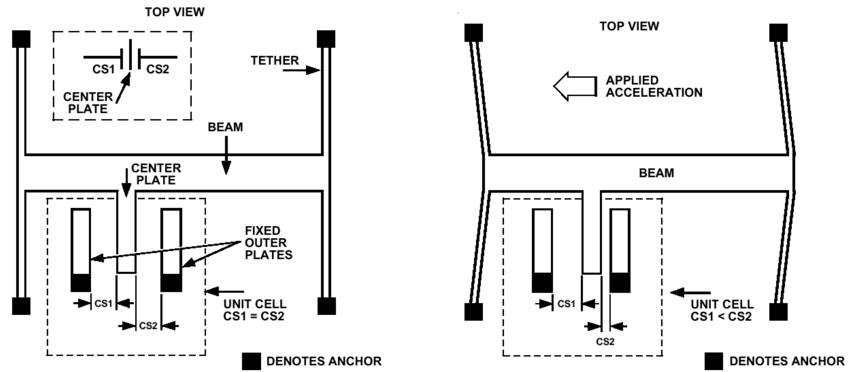
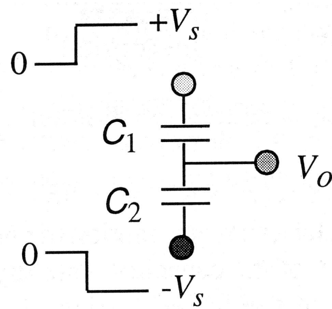
Differential Capacitive Accelerometer



Differential Capacitive Sensing



$$V_0 = \ V_s + \frac{C_1}{C_1 + C_2} \ 2V_s$$

$$= \frac{C_1 \quad C_2}{C_1 + C_2} V_s$$

$$C_1 = C\frac{x_0}{x_0 + \ x} \qquad C_2 = C\frac{x_0}{x_0 \quad x}$$

For small displacement:

$$C_1 \quad C_2 = C\left(\frac{x_0}{x_0 + \ x} \quad \frac{x_0}{x_0 \quad x}\right)$$

$$= C\frac{2x_0 \ x}{x_0^2 \quad x^2} \quad C\frac{2}{x_0} \ x$$

$$C_1 + C_2 \quad 2C$$

$$V_0 \quad \frac{x}{x_0} V_s$$

Output voltage is linearly proportional to the displacement

Introduction to Si Processing

EE143 in one day

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Silicon Device Fabrication Technology

- **Over 10^{19} transistors (or 1,000,000,000 for every person in the world) are manufactured every year.**
- **Variations of this versatile technology are used for flat-panel displays, micro-electro-mechanical systems (*MEMS*), and even DNA chips for DNA screening...**

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Foundry (Fab)

- **Foundry (also called a fab for fabrication plant) is used to refer to a factory where devices like integrated circuits are manufactured. The central part of a fab is a cleanroom.**
- **Note the difference between a fab and a lab.**

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Cleanroom Standards

Federal Standard Class Limits

CLASS	maximum particles/ft³ MEASURED PARTICLE SIZE (MICROMETERS)				
	>0.1 µm	>0.2 µm	>0.3 µm	>0.5 µm	>5.0 µm
1	35	7.5	3	1	NA
10	350	75	30	10	NA
100	NA	750	300	100	NA
1,000	NA	NA	NA	1,000	7
10,000	NA	NA	NA	10,000	70
100,000	NA	NA	NA	100,000	700

Why do we need cleanrooms?

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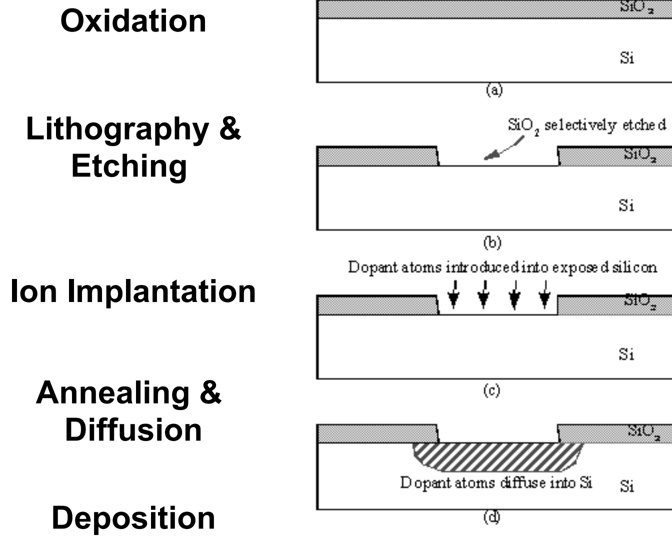
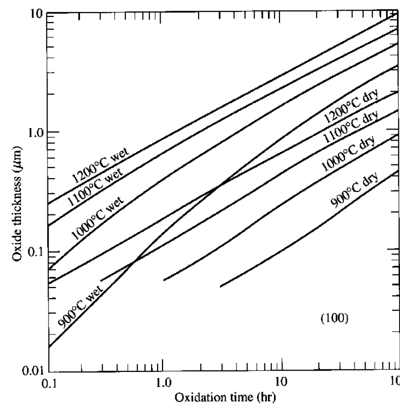
Introduction to Device Fabrication

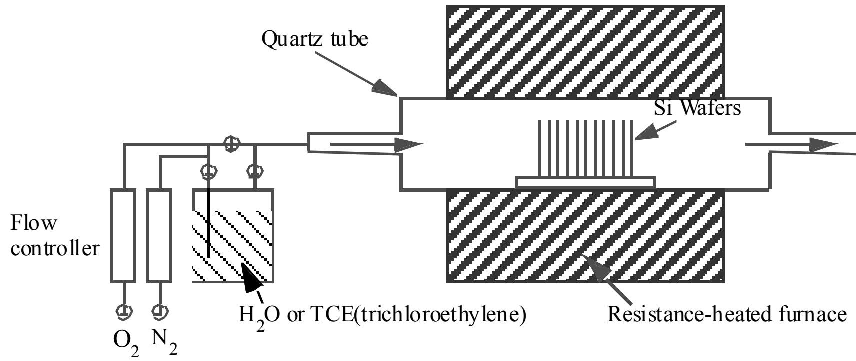


Oxidation of Silicon

Dry Oxidation :	$Si + O_2 \rightarrow SiO_2$	**Thin oxide**
Wet Oxidation :	$Si + 2H_2O \rightarrow SiO_2 + 2H_2$	**Thick oxide**



Oxidation of Silicon



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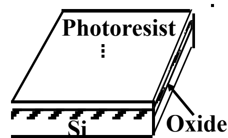
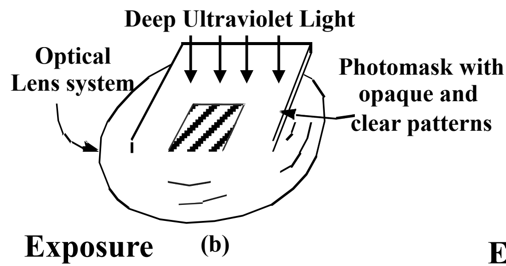
Lithography

Resist Coating



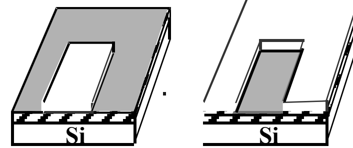
(a).



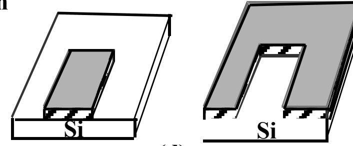
Exposure (b)

Development

Positive resist Negative resist



(c)



(d)

Etching and Resist Strip

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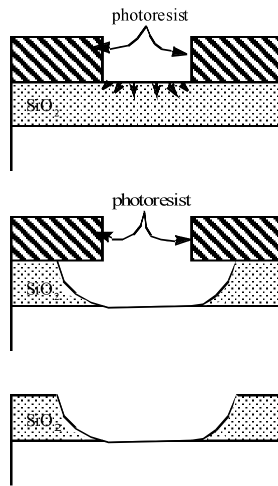
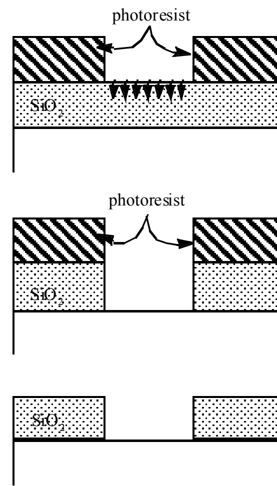
Pattern Transfer – Etching

wet etch
Isotropic etching

dry etch
Anisotropic etching





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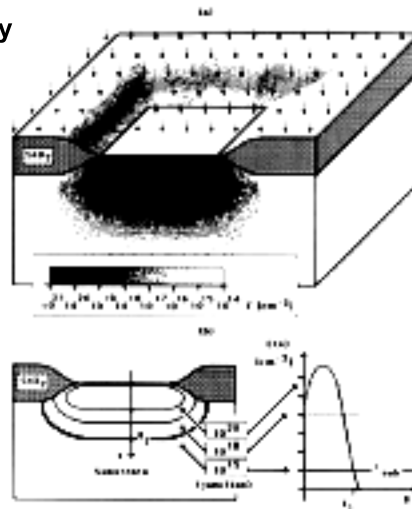
Ion Implantation

Ion Energy
~1 keV to
200 keV



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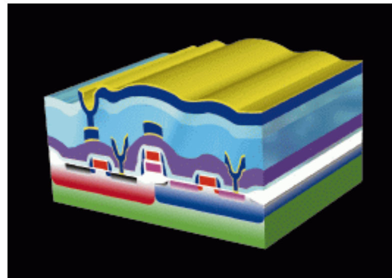
What is process integration?

- Sequential use of a series of simple process steps or "modules" to create complex structures

Processing Steps



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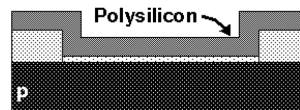
The EE143 Lab Process (part I)

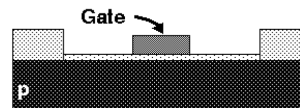
Week 2: Field Oxidation - 5200 A

Week 5: Poly-Si Deposition

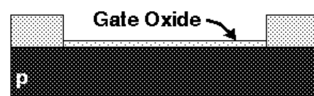


Week 3: Active Area Photolithograpl

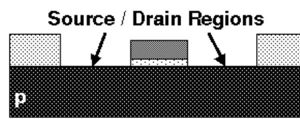
Week 6: Gate Photolithography



Week 4: Gate Oxidation - 800 A



Week 6: Clear Source and Drain



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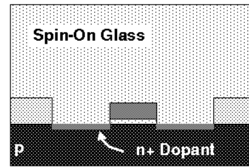
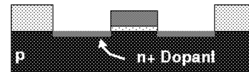
The EE143 Lab Process (Part II)

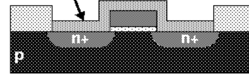
Week 7a: Source-Drain Deposition (N+)



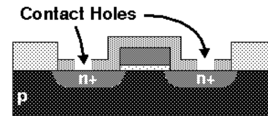
Week 7b: Spin-on Glass Strip



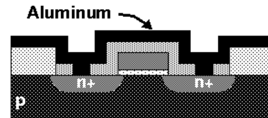
Week 7b: Drive-In Oxidation



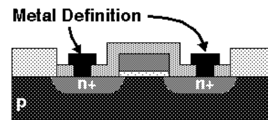
Week 8: Contact-Hole Cut (Mask #3 - CONT)



Week 9: Metallization



Week 10: Metal Definition



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