# EE143 – Fall 2016
# Microfabrication Technologies

# Lecture 14: MEMS Process


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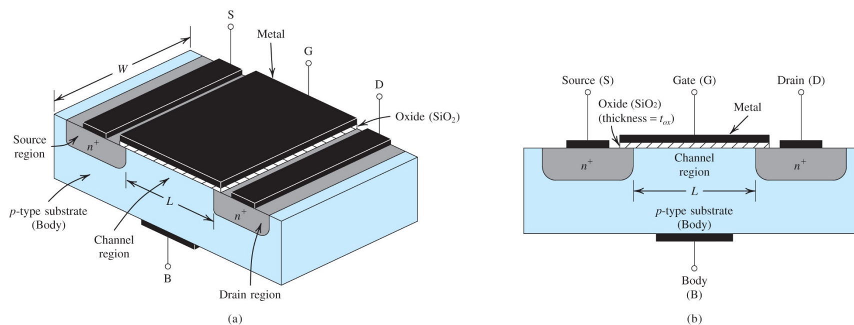
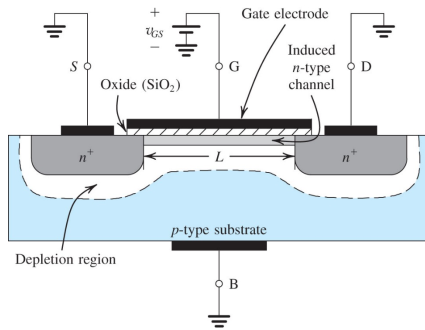
# MOSFET



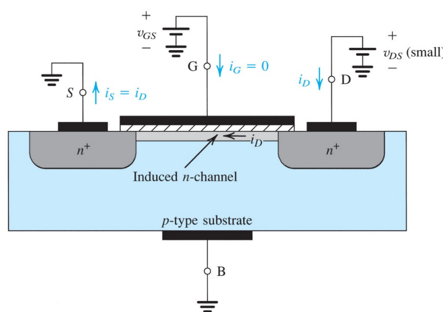

- **MOSFET: metal-oxide-semiconductor field effect transistor**
- **Typically**
  - **Channel length: L ~ 10 nm to 0.35 μm,**
  - **Channel width: W ~ 0.05 μm to 100 μm,**
  - **Oxide thickness: $t_{ox}$ ~ 1 to 10 nm**

# NMOSFET (or simply NMOS)




- N-channel MOSFET
  - Current conducted by electrons
- 3 terminal device
  - Source (S): n+ (heavily n-type)
  - Drain (D): n+
  - Gate (G): metal deposited on insulator above channel
- Substrate (called "Body") is a 4th terminal
  - Substrate is p-doped
- Electrons is induced in channel when a positive gate voltage is applied
- Electrons moves from Source to Drain
  - Current flows from D to S

# Creating a "Channel" for Current Flow




MOS is a capacitor across an insulator (oxide)
When a positive voltage is applied at Gate, electrons are induced under the gate.
At "thresold", sufficient number of electrons form a "channel" between Source and Drain, forming a conductive channel.
Total charge in the channel:

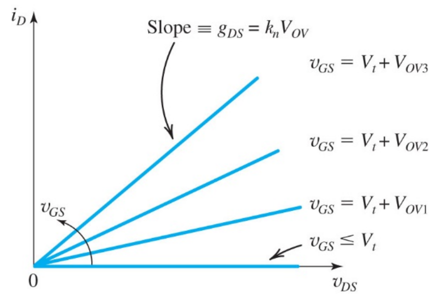
$$|Q| = C_{ox} \cdot WL \cdot (v_{GS} - V_t)$$

where $C_{ox} = \dfrac{\varepsilon_{ox}}{t_{ox}}$ is oxide capacitance per unit area

$\varepsilon_{ox} = 3.9\varepsilon_0 = 3.9 \times 8.854 \times 10^{-12}$ F/m
$W$: gate width
$L$: gate length
$V_t$: Threshold voltage

$v_{GS} - V_t \equiv v_{OV}$ is called "Overdrive Voltage"

# Current at Small $v_{DS}$




When $v_{OV} = v_{GS} - V_t > 0$, a channel is formed between Source and Drain.

Linear charge density in channel:

$$\frac{|Q|}{L} = C_{ox} W \cdot v_{OV}$$

Electric field along the channel

$$|E| = \frac{v_{DS}}{L}$$

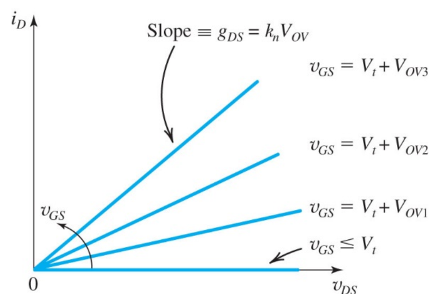
Drain current = charge density x velocity:

$$i_D = \frac{|Q|}{L} v_n = \frac{|Q|}{L} \mu_n |E| = C_{ox} W \cdot v_{OV} \mu_n \frac{v_{DS}}{L}$$

$$i_D = \mu_n C_{ox} \frac{W}{L} v_{OV} v_{DS}$$

At small $v_{DS}$, the transistor is like a gate-controlled variable resistor

# Current at Small $v_{DS}$




$$i_D = \mu_n C_{ox} \frac{W}{L} v_{OV} v_{DS}$$

$$= k_n' \frac{W}{L} v_{OV} v_{DS}$$

$$= k_n v_{OV} v_{DS}$$

where

$k_n' = \mu_n C_{ox}$ : process transconducance paramter

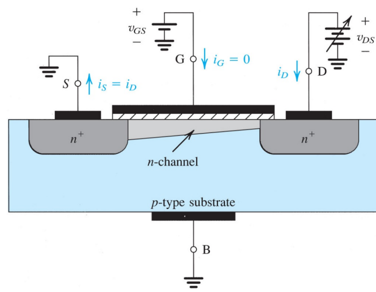
$k_n = \mu_n C_{ox} \frac{W}{L}$ : MOSFET transconductance parameter

MOSFET behaves like a linear resistor

$$r_{DS} = \frac{v_{DS}}{i_D} = \frac{1}{k_n v_{OV}}$$

Resistance value can be changed by gate voltage (overdrive voltage)

# Triode Region ($v_{DS} < v_{OV}$)




As $v_{DS}$ increases, the potential in the channel is no longer a constant. Assume the channel is $v(x)$:

$$i_D = C_{ox}W\left(v_{GS} - v(x) - V_t\right)v_n(x)$$

$$v_n(x) = \mu_n \left|E(x)\right| = \mu_n \frac{dv(x)}{dx}$$

Note: $i_D$ is still constant along the channel (think Kirchhoff's Current Law)

Integrate along the channel

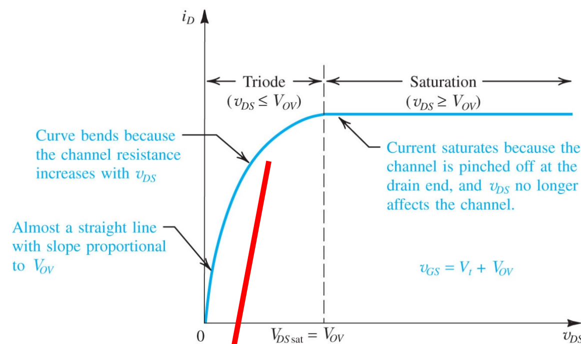
$$\int_{x=0}^{x=L} i_D dx = \int_{x=0}^{x=L} \left(C_{ox}W\left(v_{GS} - v(x) - V_t\right)\mu_n \frac{dv(x)}{dx}\right)dx$$

Change of variable on right-hand side: $x \to v$

$$i_D L = \int_{v=0}^{v=v_{DS}} \left(C_{ox}W\left(v_{OV} - v\right)\mu_n\right)dv$$

$$i_D = \mu_n C_{ox} \frac{W}{L}\left(v_{OV}v_{DS} - \frac{1}{2}v_{DS}^2\right)$$

# Triode Region ($v_{DS} < v_{OV}$)

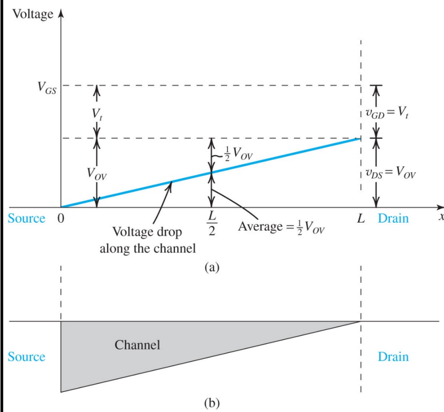



When $0 \le v_{DS} \le v_{OV}$

$$i_D = \mu_n C_{ox} \frac{W}{L}\left(v_{OV}v_{DS} - \frac{1}{2}v_{DS}^2\right)$$

This is called the "Triode Region"

# Pinch-Off




The channel potential at the drain side is $v_{DS}$.

When $v_{DS} = v_{OV}$, the local charge density there

$$\frac{|Q|}{\text{area}} = C_{ox}\left(v_{GS} - v_{DS} - V_t\right) = C_{ox}\left(v_{OV} - v_{DS}\right) = 0$$

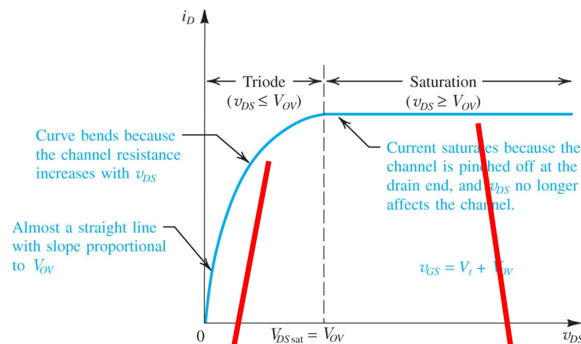
So the channel is "pinched off" near the Drain.

Once the channel is pinched off, the drain current remains constant:

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}v_{OV}^2$$

This region, $v_{DS} > v_{OV}$, is called "Saturation"

# Saturation Region ($v_{DS} > v_{OV}$)




When $0 \le v_{DS} \le v_{OV}$

$$i_D = \mu_n C_{ox}\frac{W}{L}\left(v_{OV}v_{DS} - \frac{1}{2}v_{DS}^2\right)$$

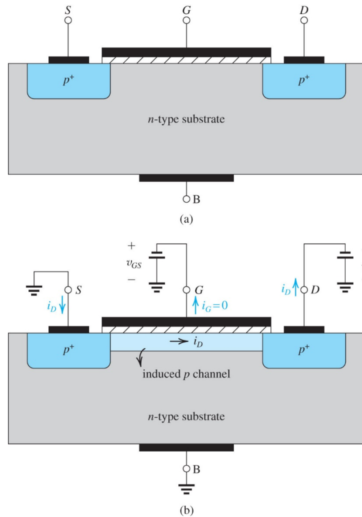
This is called the "Triode Region"

When $v_{DS} > v_{OV}$,

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}v_{OV}^2$$

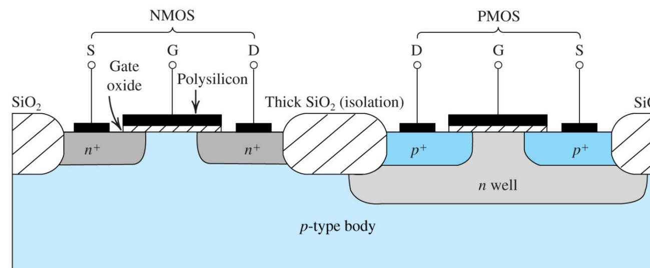
This is called "Saturation Region"

# PMOSFET (or simply PMOS)




- P-channel MOSFET
  - Current conducted by holes
- 3 terminal device
  - Source (S): p+ (heavily p-type)
  - Drain (D): p+
  - Gate (G): metal deposited on insulator above channel
- Substrate (called "Body") is a 4th terminal
  - Substrate is n-doped
- Holes is induced in channel when a negative gate voltage is applied
- Holes moves from Source to Drain
  - Current flows from S to D

# CMOS (Complementary MOS)




- CMOS is the prevalent IC technology today
- Since NMOS and PMOS are formed on oppositely doped substrates, one of the transistor needs to be placed in a "well"
- PMOS is placed in an "n well" here.
- Alternatively, NMOS can be placed in p well