EE143 – Fall 2016
Microfabrication Technologies

Lecture 14: MEMS Process

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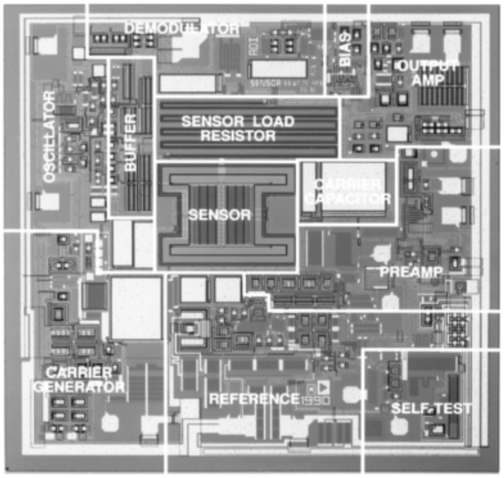
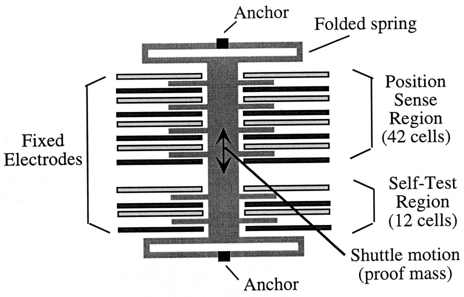
ADXL-50 Chip Diagram



Analog Devices' ADXL-50, the industry's first surface micromachined accelerometer, includes signal conditioning on chip.

ADXL Sensors



http://www.analog.com/publications/magazines/Dialogue/archives/30-4/acccel.html

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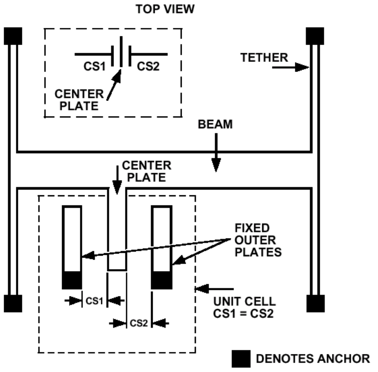
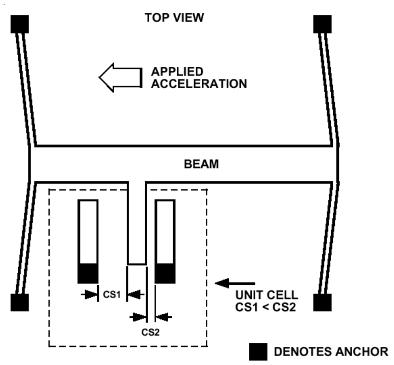
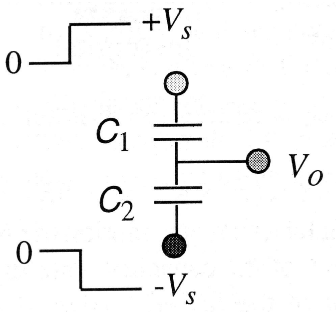
ADXL Differential Capacitive Sensor





Differential Capacitive Sensing



$$V_0 = -V_S + \frac{C_1}{C_1+C_2}\cdot 2V_S$$
$$= \frac{C_1-C_2}{C_1+C_2}V_S$$

$$C_1 = C\frac{x_0}{x_0+\delta x} \qquad C_2 = C\frac{x_0}{x_0-\delta x}$$

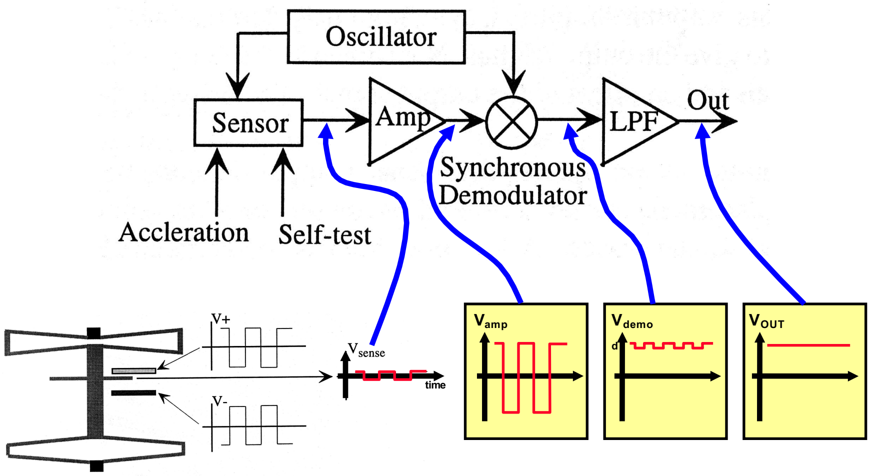
For small displacement:

$$C_1 - C_2 = C\left(\frac{x_0}{x_0+\delta x} - \frac{x_0}{x_0-\delta x}\right)$$
$$= C\frac{-2x_0\delta x}{x_0^2-\delta x^2} \approx -C\frac{2}{x_0}\delta x$$
$$C_1 + C_2 \approx 2C$$

$$\boxed{V_0 \approx -\frac{\delta x}{x_0}V_S}$$

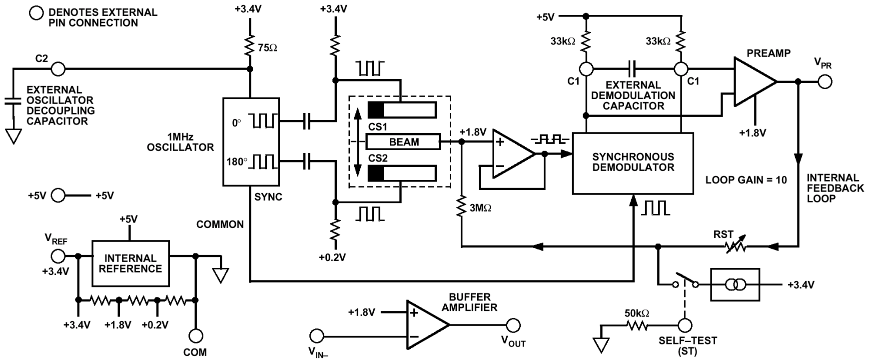
Output voltage is linearly proportional to the displacement

ADXL Block Diagram – Open Loop

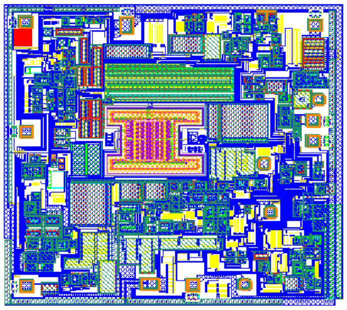


Close-Loop Force-Feedback Accelerometers -- ADXL 50 Block Diagram

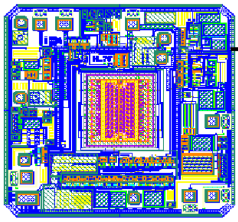
- The feedback signal is fed back to the sensing comb, keeping the combs at nearly zero displacement
- The signal = the voltage required to keep the comb at zero displacement



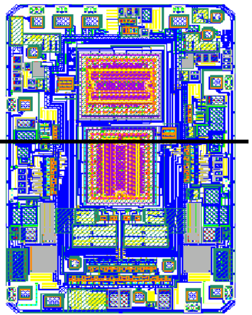
ADI's ADXL Family of Accelerometers



XL50
Original



XL150
New

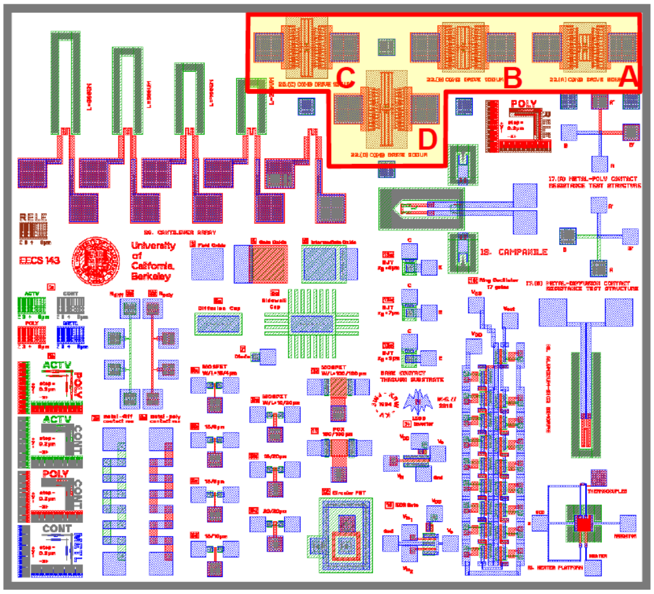


XL250
2 Channel New

Interesting facts

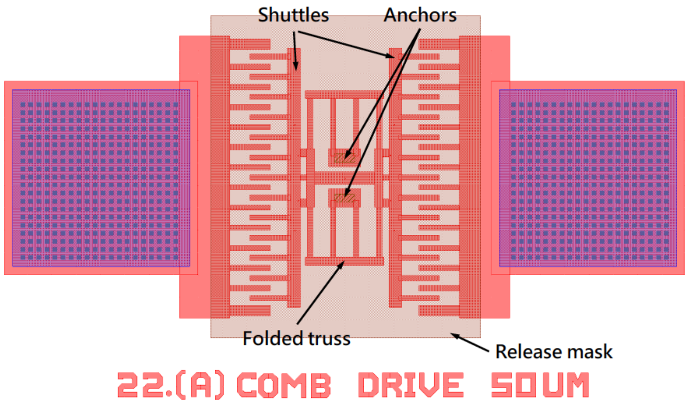
- 0.1µgrams Proof Mass
- 0.1pF per Side for the Differential Capacitor
- 20aF (10^{-18}f) Smallest Detectable Capacitance Change
- Total Capacitance Change for Full-scale is 10fF
- 1.3µm Gaps Between Capacitor Plates
- 0.2Å Minimum Detectable Beam Deflection (one tenth of an Atomic diameter)
- 1.6 µm Between the Suspended Beam and Substrate
- 10 to 22kHz Resonant Frequency of Beam

MEMS Structures in EE 143 Process



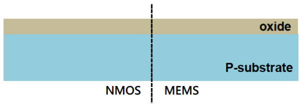
MEMS Structures in EE 143 Process

- Comb width and spacing = 5 µm
- Shuttle width = 13µm, folded truss = 12µm, anchor size = 8*20 µm^2
- Beam length = (A)50 µm, (B)100 µm, (C)150 µm and (D)200 µm

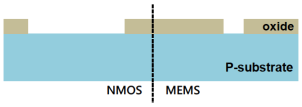


MEMS Structures in EE 143 Process

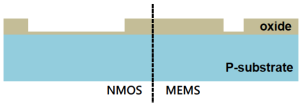
Week 3: Field oxidation (5000 Å)



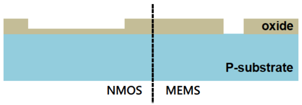
Week 4: Lithography (Mask I, Active) – define active area (NMOS) ; anchor (MEMS)



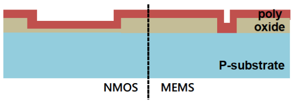
Week 5: Gate oxidation (800 Å)



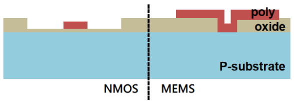
Week 6a: Lithography (Mask V, Release) – open anchor (MEMS)



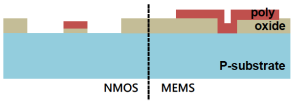
Week 6b: Polysilicon deposition (done in Microlab by TA)



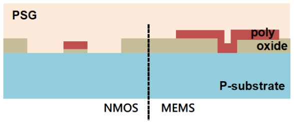
Week 7a: Lithography (Mask II, Poly) – define poly-Si gate (NMOS) and structures (MEMS)



Week 7b: Etch thin oxide – open source-drain area

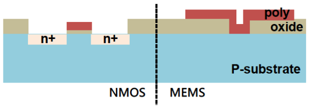


Week 8a: Source-drain (S/D) pre-deposition

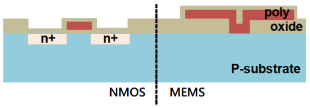


MEMS Structures in EE 143 Process

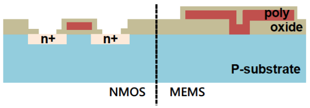
Week 8b: S/D drive-in



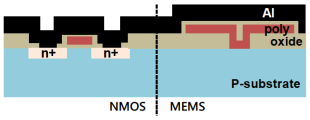
Week 8c: Intermediate oxidation (1500 Å)



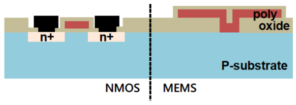
Week 9: Lithography (Mask III, Contact) – open S/D contact (NMOS)



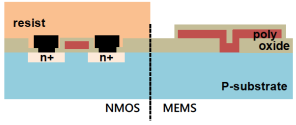
Week 10: Metallization (Aluminum evaporation: 8000 Å)



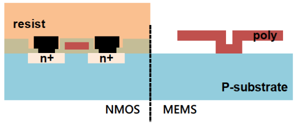
Week 11: Lithography (Mask IV, Metal) – define aluminum lines



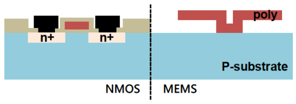
Week 12a: Lithography (Mask V, Release) – protect NMOS area



Week 12b: Release MEMS comb-drive structures in HF

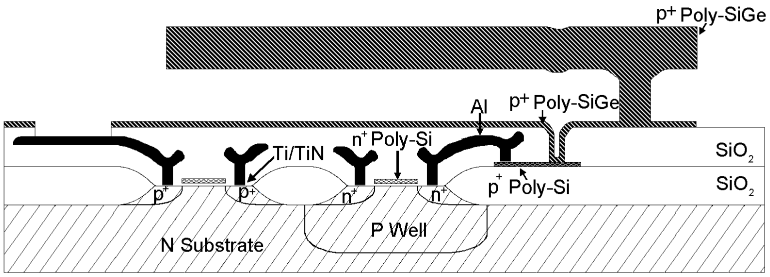


Final cross-section



$Si_{0.35}Ge_{0.65}$-MEMS/CMOS Technology

Schematic cross-sectional view of modularly integrated devices



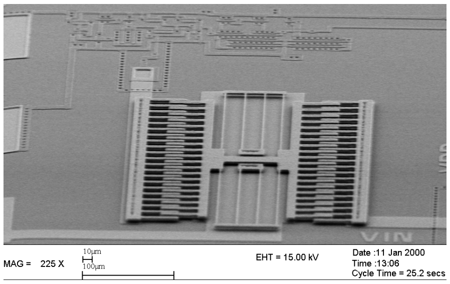
- **Conventional CMOS process (Al metallization)**
- **Structural layer: ~65% Ge, 2.5 μm thick**
  - **deposited by LPCVD at 450°C (1μm/hr), in-situ B doped (6 Ω/☐)**
  - **no post-dep. anneal (-10 MPa stress; ~10^{-4}/μm strain gradient)**
- **Sacrificial layer: 100% Ge, 2 μm thick**
  - **deposited by LPCVD at 450°C (~1 μm/hr)**
  - **selectively removed using H_2O_2 (80°C) to release microstructures**

T.-J. King-Liu, R. Howe

Integrated SiGe-MEMS/CMOS

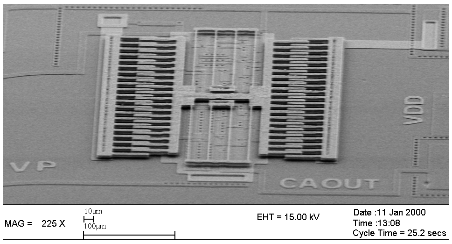
Resonator next to Amplifier

- conventional layout of integrated MEMS



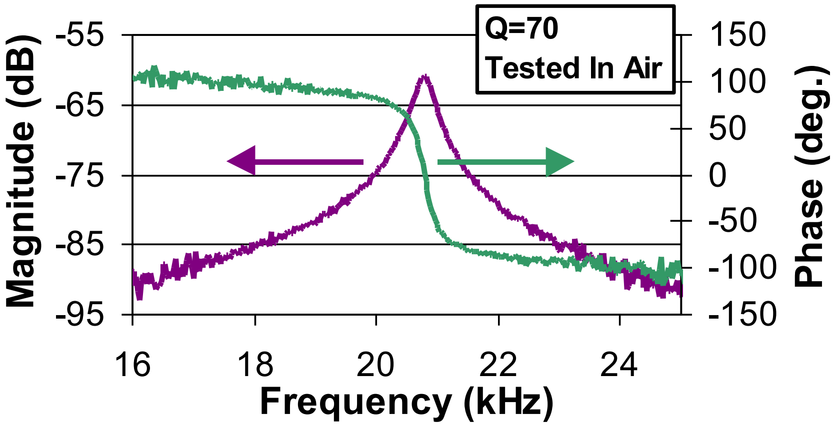
Resonator on top of Amplifier

- smaller area --> lower cost
- reduced interconnect parasitics --> improved performance



A. E. Franke *et al.*, *Solid-State Sensor and Actuator Workshop Technical Digest*, pp. 18-21, June 2000

$Si_{0.35}Ge_{0.65}$ Resonator Response



Q = 14,000 at 40 μTorr