Week 8 Student Checklist
Modified: Shong Yin, Spring 2006

Student checklist

- Review the overall Process Flow. This can be found at the lab webpage: http://www-inst.eecs.berkeley.edu/~ee143/sp06/lab/fabrication_process_flow.pdf
- Read the detailed Process Flow for week 8 available on the lab web site at: http://www-inst.eecs.berkeley.edu/~ee143/sp06/lab/NMOS-process-flow.pdf
  Week 8: Contact Cut. Please read through the process step in detail and you should understand how to ensure complete opening of the contact holes, without causing shorts to the gate layer.

  NOTE: WE ARE ALMOST THERE! The devices have now been made. We need to make the metal contacts to them so that we can make measurements. This lab is very critical in the sense that if the contact hole is not completely opened and if the oxide is not completely removed, then all you have done till now cannot be "electrically accessible" and therefore, can get wasted.
- To review lithography, please look at the Lithography Module Video available online at:
  http://www-inst.eecs.berkeley.edu/~ee143/sp06/lab.html
  Link: EE143 Lab: Lithography module video
- It is a usual lithography step, but the alignment is the hardest of all the lithography steps we have done till now. Go through the mask layout and think about what to expect. Note: It is a dark field mask and seeing the wafer below is difficult.
- Go through the Quintel Mask Aligner Manual at: http://www-inst.eecs.berkeley.edu/~ee143/sp06/lab/Quintel.pdf. Review the alignment procedure and get an idea of what alignment problems you will face in the lab.
- Review the Vernier Tutorial to measure your misalignment. This is available at: http://www-inst.eecs.berkeley.edu/~ee143/sp06/lab/vernier.pdf
- Print out and complete the Week 8 Quiz from the lab web page, before coming to your lab session.