# LAB REPORT 1

***Due: Friday, Apr. 23, 2010*, 7:00 p.m. in the EE 143 homework box in 240 Cory**

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**I. Profiles & Layout (14 Points)**
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***Total Points = 110 possible (graded out of 100)***

**Please be sure to include the requirement signature regarding academic honesty. All lab group members should print out this page (the last page after the report template), sign on the attached form, and include it with your Lab Report. Thank you!**

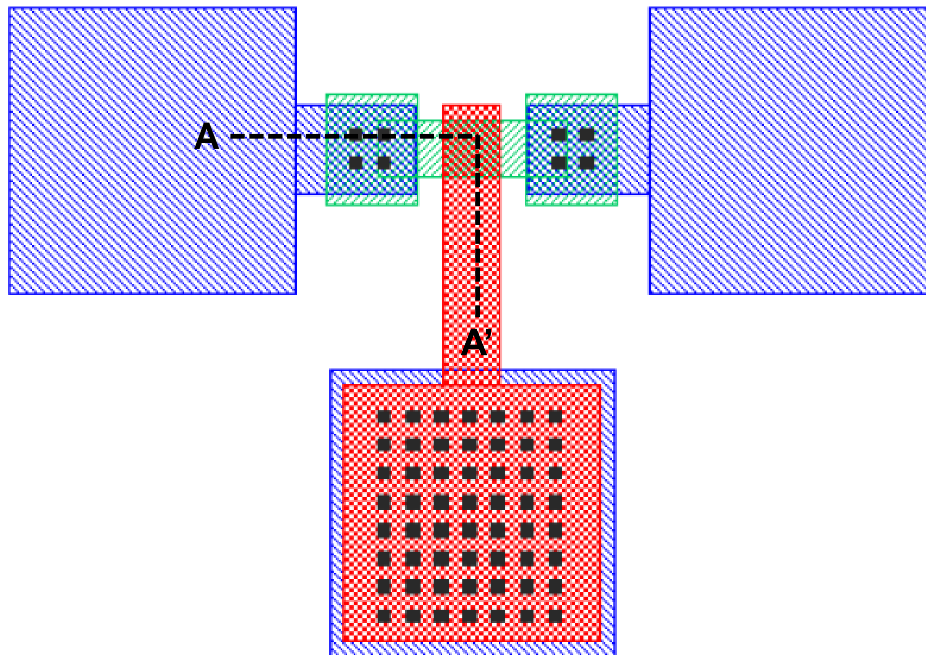
**REPORTS MUST BE WORD PROCESSED (EXCEPT FOR SKETCHES AND HAND WRITTEN CALCULATIONS)**

**Each group of students will submit one joint report. There will be a 20 PAGE max limit on the report. Please use the report template. Profiles & Layout and Calculations do not count towards this page limit. *FOLLOW THE ATTACHED TEMPLATE FORMAT FOR THE REPORT. STUDENTS NOT FOLLOWING THIS FORMAT WILL BE DEDUCTED 10% PER SECTION DEVIATING FROM TEMPLATE.* When possible, be concise and use structured bullet points!**

## I. Profiles & Layout (14 Points)

The process flow:

W1: Staring Wafer
W2: Field Oxidation
W3: ACTV Photolithography and Etch
W4: Gate Oxidation
W5a: Anchor Opening Photolithography for MEMS
W5b: Polysilicon CVD
W6: POLY Lithography and Etch, Source/Drain Clear
W7a: Spin-on Glass + Source/Drain Pre-diffusion
W7b: Source/Drain Drive-in + Intermediate Oxidation
W8: CONT Photolithography and Etch
W9: Aluminum Evaporation
W10: METL Photolithography + Etch
W11: RELE (MEMS Comb-drive Structure Release) Photolithography + Etch




Draw cross-sectional profiles *AA'* of a *MOSFET* (test structure #9) after each of the steps:

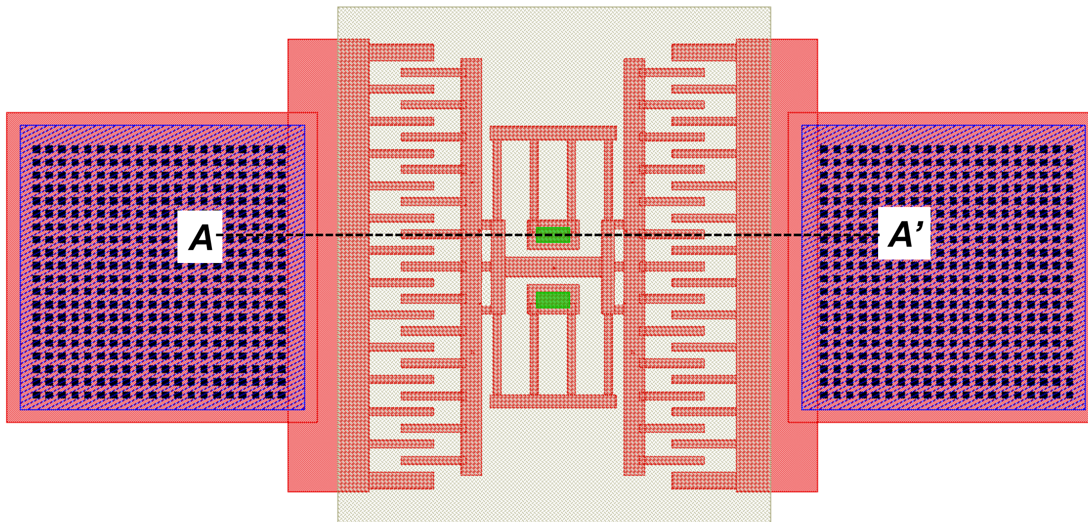
Indicate all layers. Label each feature and indicate thicknesses (make roughly proportional sketches). Illustrate and describe important details:

- non-planar interfaces from thermal oxidation
- isotropic etch profiles
- point-source Al evaporation
- thermal oxidation growth

These drawings should have significantly more detail than those on the lab manual website. See the diagram below for the exact cross-sections in question. (5 Points)

B. Draw top views of the same thin-oxide *MOSFET* (test structure #9) after each of the four photolithography steps. [ACTV, POLY, CONT, METL] (4 Points)

C. Draw cross-sectional profiles of the comb-drive (*MEMS* - test structure #22) after each of the 12 major processing steps, in the same fashion that you did for the MOSFET. See the diagram below for the exact cross-sections in question. The line runs through the anchor hole of the polystructure. (5 Points)




**II. Process Procedures (20 Points) [Refer to Template at the back of the Report]**

A. Describe monitoring measurements that were done during processing:

Film color
Line Width
Thickness

Resistivity
Vernier

Determine whether each layer was overetched or underetched? Did you purposely over/underetch? Why?

Describe how the verniers are used to measure misalignment. Using diagrams may help. Were any layers misaligned intentionally? For each pair of verniers (ACTV-POLY, ACTV-CONT, POLY-CONT, CONT-METL, POLY-RELE), describe how far the marks may be misaligned in terms of device function. (6 Points)

B. List and concisely describe the possible problems that could have occurred during the batch fabrication steps:

W2: Field Oxidation
W4: Gate Oxidation
W5: Poly Deposition
W7a: Source-Drain Prediffusion
W7b: Drive-In & Intermediate Oxidation
W9: Aluminum Evaporation
W10: Sintering

What were the sources of the problems, and how could you avoid them? How do you expect these deviations to affect the performance/function and cross-section of the device? List the types of monitoring measurements from Part A taken during each step (7 Points)

C. Other than the problems that occurred during the batch sessions, what were the particular problems (or deviations from other groups) that could occur in YOUR wafer? Specifically these are the steps where all wafers were run in individually.

W3: ACTV Photolithography
W5: ANCR (anchor opening for MEMS) Photolithography
W6: POLY Photolithography
W7: SOG Deposition & SOG Strip
W8: CONT Photolithography
W10: METL Photolithography
W11: RELE (protect MOSFET for MEMS release) Photolithography

What were the causes and how were the problems overcome? How would these affect device performance? Include any illustrations that would be helpful. List the types of measurements from Part A taken during each step (7 Points)

## III. Calculations (36 Points) [Refer to Report Template at Back of Report]

Fill the template table with the following parameters from your own wafer: (3 points)

a) Film thickness (each layer)
b) Sheet Resistance (after ion implantation and S&D formation)
c) % over/underetch measured photoresist from theoretical (each layer)

Calculate the parameters asked for in the following questions—list both the theoretical values and the empirical values, when applicable. We would like to see that you understand what processing abnormalities may have led to a discrepancy between the two. Neatly write up and annotate all calculations and attach in appendix. (Points will be deducted if we cannot understand what you wrote).

1. Theoretical and experimental thicknesses of field oxide, gate and intermediate oxides (Include orientation dependence of oxidation rate but not impurity dependence) (9 points)
2. Junction depths after pre-diffusion and drive-in (theoretical, assume only phosphorous doping with surface concentration limited by solid solubility). You must consider the effect of the initial ion implantation. For pre-deposition you may use the box approximation, but for drive-in you must use the half-gaussian calculation. Why is this? (10 points)
3. Final surface concentrations of dopants, as determined from Irvin's curves using sheet resistance measurements made in lab. (2 points)
4. Plot or sketch the change of dopant profile from the silicon surface through the source-drain after each thermal step.

    - Field Oxidation
    - Gate Oxidation
    - Poly-Deposition
    - Pre-Deposition
    - Drive-In & Intermediate Oxidation.
    - Sintering

    Quantitatively label significant points such as Peak concentration, Peak Width, Junction Depth. Show movement of the Silicon-Silicon Dioxide interface and qualitatively show non-ideal effects such as dopant redistribution during oxidation. (11 points)
5. Lateral diffusion under the MOSFET gates. You may estimate. Justify estimation. (Theoretical). (2 points)
6. List an estimate of the Young's modulus, Poisson ratio, and coefficient of thermal expansion for $SiO_2$, poly-Si, and Al films as deposited. (You can find these in a table in many physics/ME textbooks, or in a web-based search.) (2 points)

**IV. Questions (30 Points - 2 points each) (3 Page Limit)**

Answer these questions in the most concise manner possible. A few lines should suffice for each.

1. What is the purpose of baking the wafers at 120°C before depositing HMDS? What is the purpose of depositing HMDS in the HMDS blue box before spinning photoresist? What is the purpose of the 90°C bake after spinning photoresist? What happens if the soft bake is too hot and too long (say 120 °C, 5 minutes)?
2. What is the purpose of the hard bake during lithography? What happens if we skip this step? What might happen if the bake is done at a temperature above 120 °C (say 200 °C)?
3. Why do we do lithography steps under yellow light only? What if we expose them to fluorescent light after development? Would red light damage your process?
4. What is the purpose of dipping wafers in DI wafer for 10 seconds before etching oxide in BHF?
5. Why is 5:1 BHF (5:1 $NH_4F$:HF) used for etching features in the oxide while 10:1 BHF is used for cleaning and spin-on-glass stripping? Why buffered HF?
6. Suppose you saw metal peeling off after the metal evaporation step. Why did this happen?
7. Why do you need to push/pull the quartz boat slowly when taking wafers into/out of the furnace? What is the purpose of turning on $N_2$ flow after an oxidation step is done?
8. Why do you strip the SOG before drive-in? What would happen if the SOG is left on the wafers during the drive-in step?
9. How does the film thickness variation affect the estimation of etch time? Did you experience any problem in the etching process due to the thickness variation?
10. What would happen if we skipped the HF dip before metallization?
11. What is the Al etchant composed of? What happens if you use it at room temperature? What is the purpose of sintering? What would happen if the sintering step were skipped? What happens if the sintering temperature is too hot? Too low?
12. How should the mask set be changed if we used lift-off to pattern the metal lines? Why didn't we use lift-off to define the aluminum interconnects?
13. What would happen if we skipped the MEMS anchor opening lithography step in week 5?
14. Describe briefly how the Nanospec measures film thicknesses. Use diagrams to help in your explanation.
15. Describe briefly how the Four-point probe measures sheet resistance. Again, you should use diagrams to explain this.

## V. Bonus Questions (up to 10 Points)

1. Identify those masks involved with making the MEMS comb-drive structures and those not involved. How many masks were actually required to make the MEMS

device? If you were required to make a suspended MEMS structure anchored to the substrate, like the one in this process, could you achieve such a structure using a single mask? How? Generate a new process flow that simultaneously achieves 1-mask MEMS comb-drive structures together with NMOS devices, describe how you would change the layout of the comb-drive device to accommodate this flow, and draw relevant cross-sections like those on the lab manual website.

2. Describe an alternate method for doing one of the process steps (i.e. LOCOS instead of Field Oxide, Sputtering instead of Evaporation, etc) and the tradeoffs.