Dopant Redistribution During Oxidation

- This must be considered and designed for when generating any process flow, especially for transistor circuits, e.g., CMOS
- During oxidation, the impurity concentration at the Si-SiO_2. interface can increase (pile-up) or deplete, depending upon the dopant type
- Whether a particular impurity depletes or piles up @ the interface depends on:
  1. Diffusion coefficient, D (of the impurity in SiO_2)
  2. Segregation coefficient, m: → if m = large → dopants want to stay in Si

$$m = \frac{\text{impurity equil. conc. in Si}}{\text{impurity equil. conc. in SiO}_2}$$

→ if m = small → dopants want to be in SiO_2

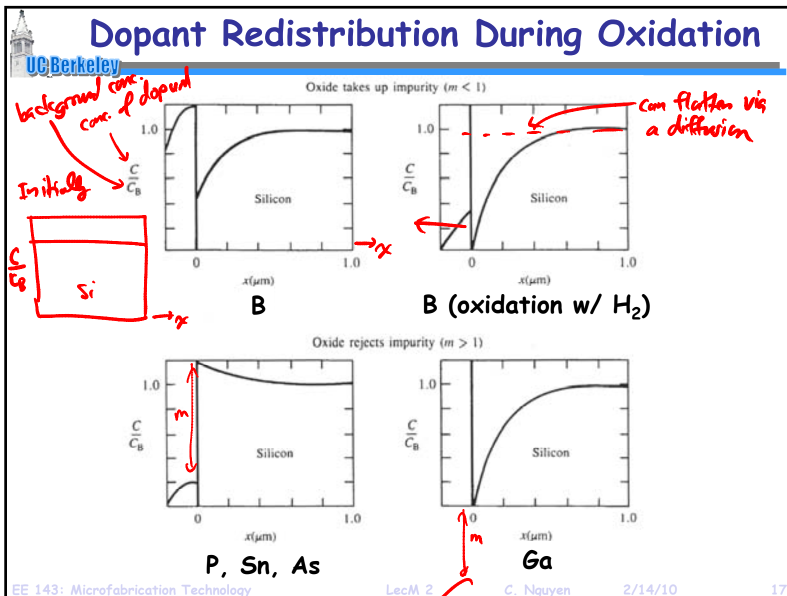
Dopant Behavior During Oxidation

- Segregation coefficient (m) and diffusion constant (D) combine to determine dopant behavior during oxidation:

Impurity	m	D in SiO_2	Dopant Behavior During Oxidation
B	<0.3 (small)	Small	depl. f/Si surface, pile up in oxide
B (oxidation w/H_2)	<0.3 (small)	Large	depl. f/Si surface, depl. from oxide
P, Sn, As	~10 (large)	Small	pile up in Si, very little diff. into SiO_2
Ga	20 (large)	Large	depl. f/Si, depl. from oxide

e.g., wet oxidation where H_2 is present as a by-product.

So large that it depletes the dopant @ the Si surface despite



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