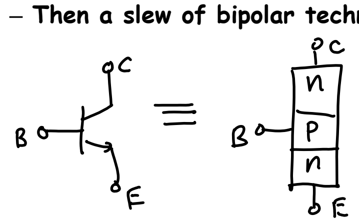
Lecture 1: Administration & Overview; History of IC's

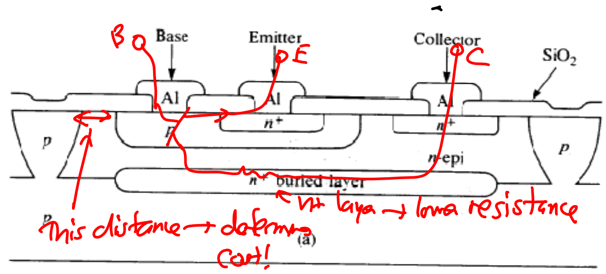
Administration & Overview

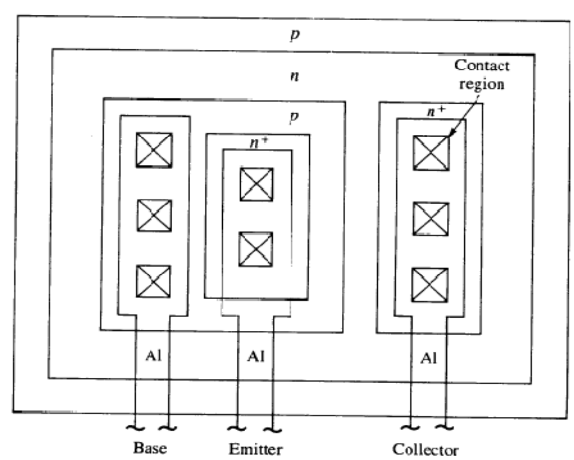
- This Lecture: Administration & Overview
- Reading: Handouts
- Lecture Topics:
  - Course information
  - Syllabus
- ---
- Welcome to EE 143: "Microfabrication Technology"
- This is our course on wafer-level fabrication of transistor integrated circuits and other micro-devices, such as MEMS
  - ☐→ Pass out course info sheet
  - ☐→ Pass out course syllabus
  - ☐→ Lab juggling; get info on the order of people signing up for labs, then only make those who were last in a section that is full move; must show data on lab section counts on first lecture sheet
  - ☐→ Show calendar and settle the office hours
- ---
- Goals of the course:
  - Teach the skills needed to design and fabricate micro- and nano-devices, including integrated circuits and micro electromechanical systems (MEMS)
  - Design emphasis: This is NOT a survey course; you will be expected to design and layout physical MOS devices (and MEMS devices, if there's time)
  - Hands-on emphasis: Give you actual hands-on experience fabricating micro-devices using a wafer-level process in a cleanroom
- The mechanics of the course are summarized in the course handouts, given out in lecture today
  - Course Information Sheet
    - → Course description
    - → Course mechanics
    - → Textbooks
    - → Grading policy
  - Syllabus
    - → Lecture by lecture timeline w/ associated reading sections
    - → Midterm Exam: Thursday, March 18 (tentative)
    - → Final Exam: Monday, May 10

IC History & Review of Devices

- Reading: Jaeger, Chpt. 1
- Lecture Topics:
  - History of IC's
  - Devices of Interest
    - → MOS transistor
    - → Micromechanical structure
- ---
- History of IC's:
  - 1834: Difference Engines (mechanical computers)
    - → Gears, cranks, levers, decimal, pipelining!
  - 1904: Vacuum tube invented
    - → Yielded the ENIAC vacuum tube computer
  - 1925: J. Lilenfield proposed the MOSFET transistor
    - → Problem: knowledge of materials not sufficient to get this to work
  - (instead)
  - 1947: Invention of the transistor (Bardeen, Brattein, Shockley)
  - 1949: Invention of the Bipolar Xsistor (Shockley)
  - 1956: First digital logic gates (Harris)
  - 1959: Invention of planar silicon processing (Kilby, Noyce)
  - Then a slew of bipolar technologies



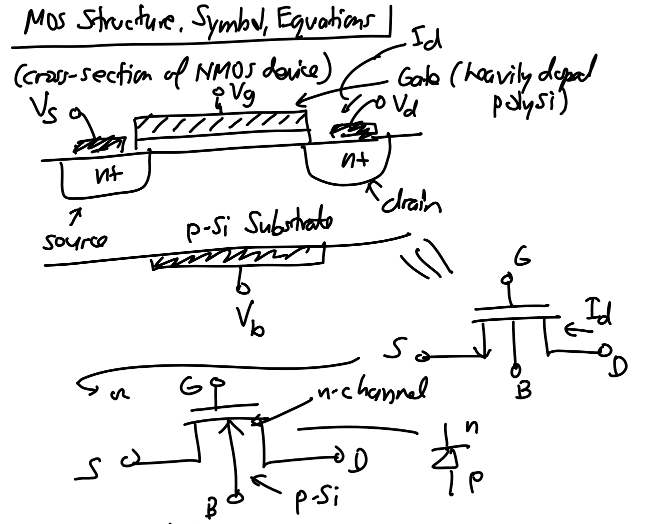




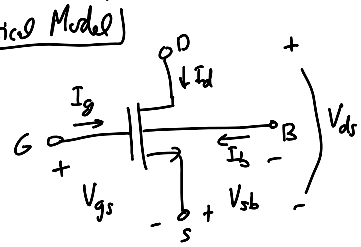
Copyright @ 2009 Regents of the University of California

- → TTL (1965)
- → ECL (1967)
- → MTL/I^2L (1972)
- → SiGe heterostructures (1990's)
- – Bipolar ruled during the 60's and 70's, because it was faster than anything else, incl. MOS
- – But soon, its excessive power consumption caught up, and MOS began to come into favor as small channel lengths boosted the speed of MOS

MOS Structure, Symbol, Equations



Mathematical Model



① Cut-Off Region: ($V_{gs} \le V_t$)

$$I_g = I_b = 0;\ I_d = 0$$

② Linear (or Triode) Region: ($V_{gs} - V_{tn} \ge V_{ds} \ge 0$)

$$I_g = I_b = 0;\ I_d = \mu_n C_{ox} \frac{W}{L}\left(V_{gs} - V_{tn} - \frac{V_{ds}}{2}\right)V_{ds}$$

$$= k_n\left(V_{gs} - V_{tn} - \frac{V_{ds}}{2}\right)V_{ds}$$

③ Saturation Region: ($V_{ds} \ge V_{gs} - V_{tn} \ge 0$)

$$I_g = I_b = 0;\ I_d = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{tn})^2(1 + \lambda V_{ds})$$

$$= \frac{1}{2}k_n(V_{gs} - V_{tn})^2(1 + \lambda V_{ds})$$

where: $\mu_n \triangleq e^-$ mobility in the channel

$C_{ox} \triangleq$ gate oxide capacitance per unit area

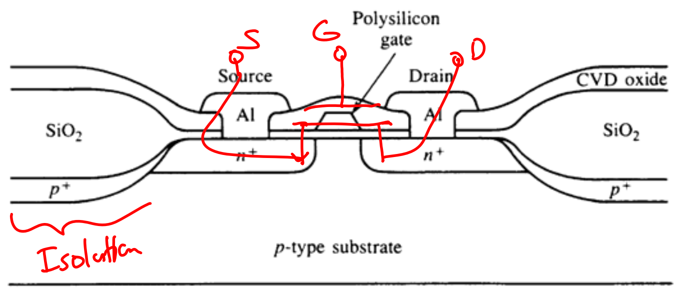
$k_n = k_n' \frac{W}{L} = \mu_n C_{ox} \frac{W}{L}$

$I_g = I_b = 0$ for all regions (at least for dc)

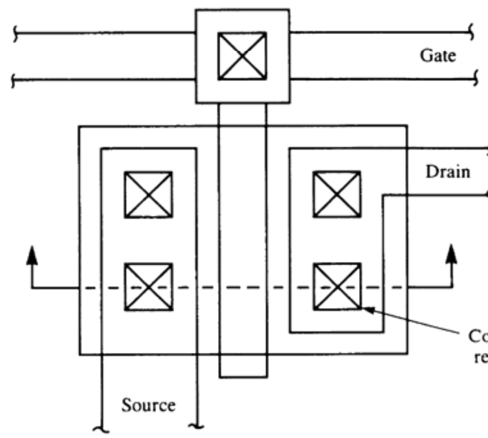
$$V_{tn} = f(V_{SB}) = V_{tn0} + \gamma\left(\sqrt{V_{SB} - 2|\phi_F|} - \sqrt{2|\phi_F|}\right)$$

Body Factor → $\gamma = \frac{1}{C_{ox}}\sqrt{2q\epsilon_s N_{sub}}$ ← substrate doping conc.

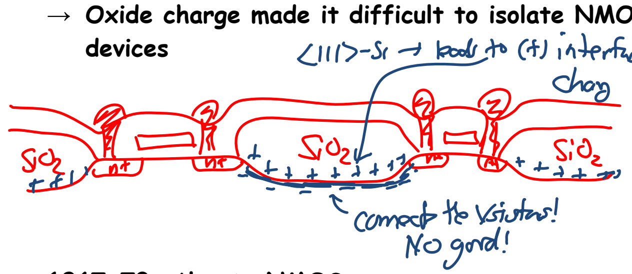
NMOS Device Cross-Section



(a)

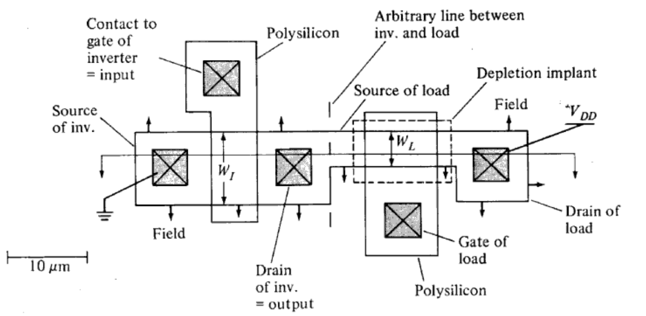


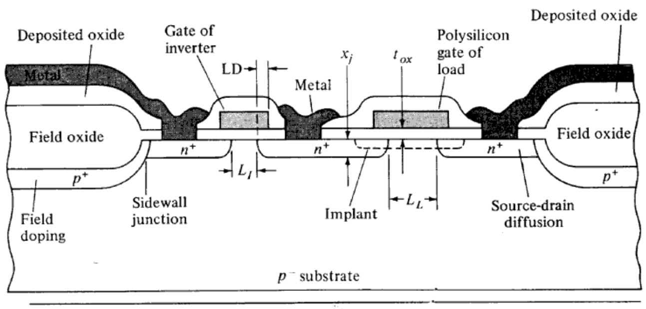
- – Fairly simple process: only 5 masks; note that this is much smaller than today's proess, which might have more than 28 masking steps
- – The rise of MOS occurred in steps:
- – 1965: PMOS w/ Al gate
  - → Used <111> wafers because bipolar used them
  - → This forced the use of PMOS, since oxide charge was dense in <111>-Si to oxide interfaces
  - → Oxide charge made it difficult to isolate NMOS devices



- – 1967-70: Al gate NMOS
  - → Use of <100>-Si together with sintering reduced oxide charges
  - → Speed faster than PMOS and path to matching bipolar speed could be seen

Copyright @ 2009 Regents of the University of California





– 1970: Si-gate NMOS
  → Advantage: self-alignment of source & drain
  → Problem: power consumption (similar to bipolar)
– To reduce power consumption, a complementary device was needed
– This is where CMOS looked advantageous

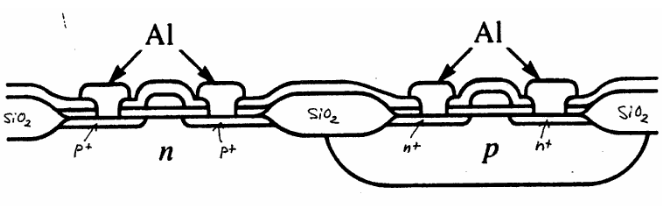
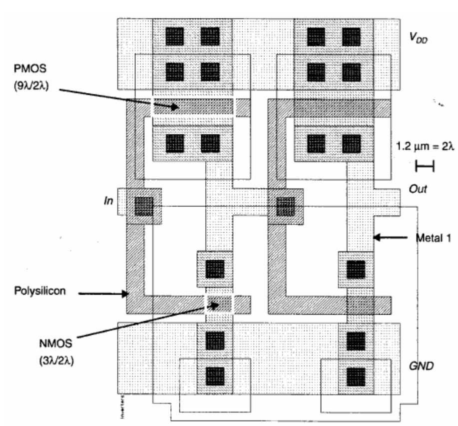


Fig. 2.1



– 1963: pwell CMOS
  → CMOS gate actually came before NMOS or PMOS, but poor control of oxide quality at the time prevented it from thriving
  → Why didn't CMOS thrive in 1963?
    1. Higher fabrication cost.
    2. Latch-up problems.
    3. Lower packing density due to need for wells.
    4. CMOS slower than NMOS due to larger gate capacitance.
– But soon power became an issue:
– 1971: Intel 4004 4-bit microprocessor
  → 2,300 devices (PMOS)
– 1978: Intel 8086 16-bit microprocessor
  → 29,000 devices (NMOS); power dissipation beginning to get up there: 1.5W @ 8MHz
– 1985: Intel 80386
  → 275,000 devices → NMOS light bulb!
  → A low power technology was needed
– Result: CMOS takes over
  → Intel 80C86 (CMOS version of 80386)
  → Intel 80486: 1.2 million Xsistors
  → Intel Pentium (P5): 3 million Xsistors
  → Intel P6: 5.5 million Xsistors in core, 15 million more in secondary cache
  → And of course it keeps going to today …
  → Intel Core 2 Duo: 820 million Xsistors
  →

Copyright @ 2009 Regents of the University of California