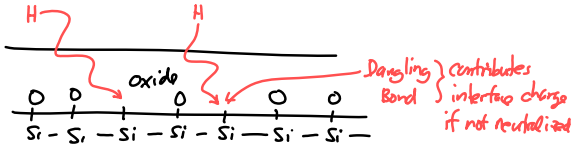
Sintering

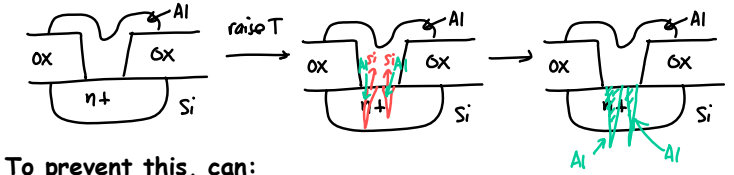
- Usually need a forming gas anneal @ 400-450°C (called sintering) at the end of an NMOS or CMOS process
  - Forming gas = mixture of H_2 and N_2
  - Improves the metal to silicon contact
  - Reduces the oxide interface charge, allowing the threshold voltage to be the right value
  - The H_2 ties up dangling bonds that would otherwise contribute fixed interface charge



- If you finish an MOS process and your thresholds are off, don't despair – just do a sintering step & this will probably fix your problems (almost like magic)

Al Spiking & Junction Penetration

- Problem: taking the temperature up too high causes silicon to diffuse into Al
  - Supply of Si tends to come from a few points, that then leave caves that Al can then go into to form spikes
  - This happens because the silicon wants to diffuse into the Al till it reaches its solid solubility limit of 0.25-1.5%



- To prevent this, can:
  - Incorporate Si into the Al so that it's closer to its solid solubility limit – usually add 1% Si to the Al target in sputtering
  - Use a barrier metal (e.g., TiW)
  - Use a barrier silicide

Contact Resistance

- Definition: Resistance associated with the contact between two materials
- Inversely proportional to the area of the contact

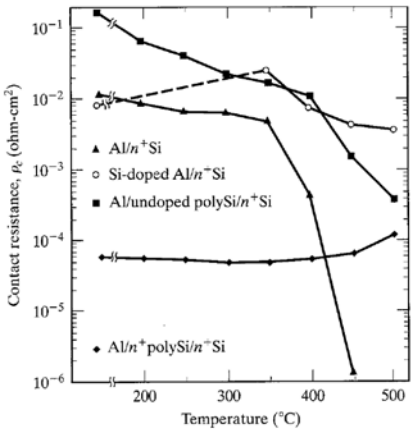
Specific Contact Resistivity [Ω·cm²]

Contact Resistance

$$R_c = \frac{\rho_c}{A}$$

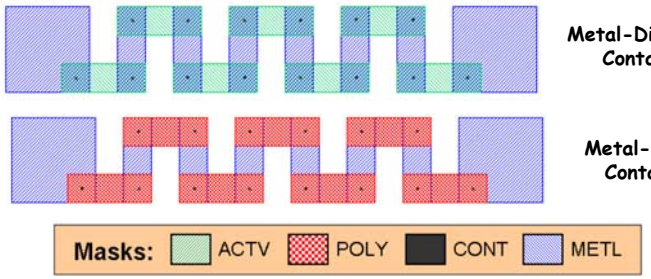
Contact Area

- Strong function of the sintering temperature



Measuring Contact Resistance

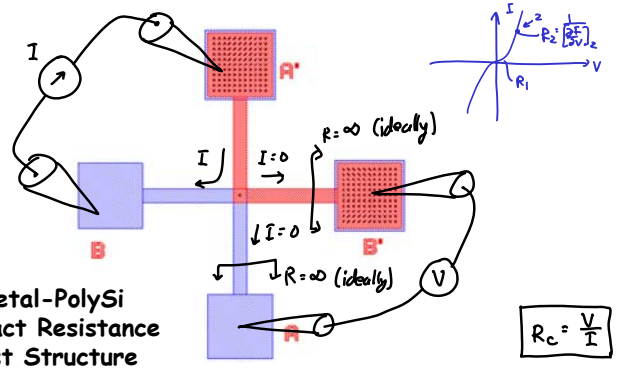
- Your lab layout includes contact chains:



- Each chain: 14 series contacts and 7 series resistive pads
- Strategy: if one uses enough contacts, the contact resistance becomes large enough to measure
- Problem: segment resistance also rises; how can one delineate the contact resistance?

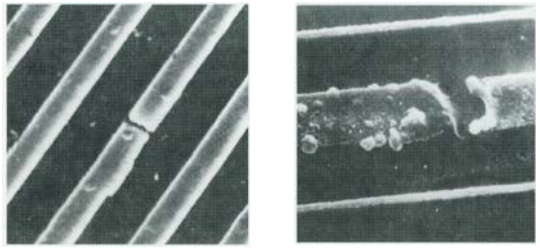
Measuring Contact Resistance

- Solution: use a 4-pt. probe strategy (also on the layout)



Electromigration

- Definition: The movement of atoms in a metal film due to momentum transfer from the electrons carrying the current
  - Happens under high current density



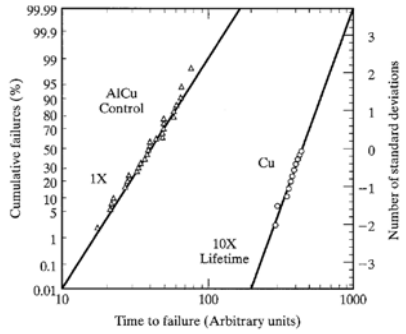
- Mean time to failure (MTF) formula:

$$MTF \propto J^{-2} \exp\left[\frac{E_A}{kT}\right]$$

where
J = current density
E_A = activation energy (0.4-0.5eV for Al)

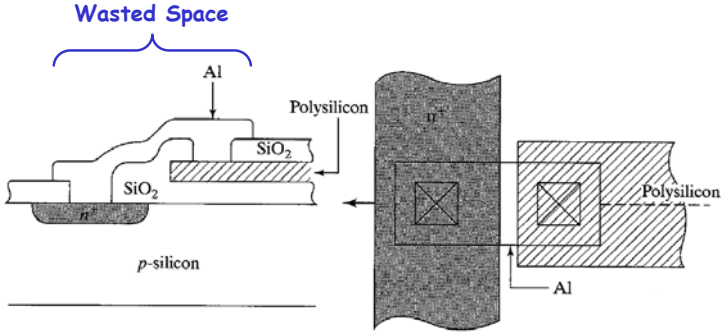
Electromigration

- To reduce electromigration can add a small percentage of a heavier metal, like Cu (to Al)
  - Cu has higher mass ⇨ more resistant to electromigration
  - Targets composed of 95% Al, 4% Cu, and 1% Si often used in sputtering systems



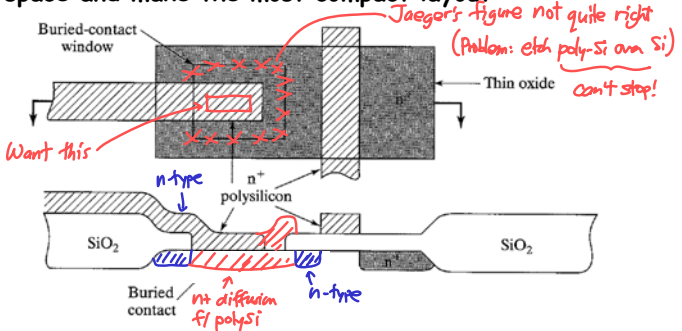
Issue: Polysilicon-to-Metal Contact

- Polysilicon-to-metal contact takes up space
- Need to eliminate waste of space for the smallest circuits, like memory arrays
- Below: conventional layout



Buried Contact

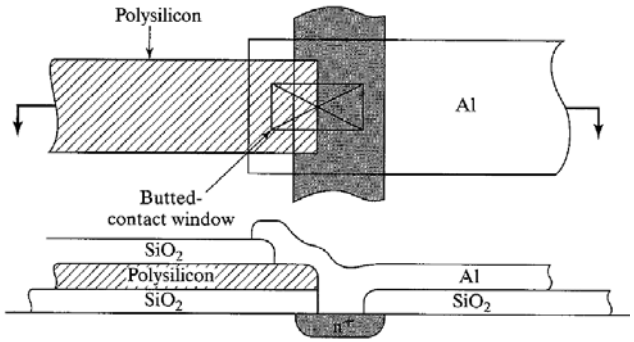
- Need to add a mask to allow a buried contact, but it can save space and make the most compact layout



- Diffusion from the n+ polySi merges with the S/D diffusion around the gate (the diffusion cannot be initially below the gate, since the gate serves as a mask against the source/drain implant)

Butted Contact

- Saves area, since it only needs one contact to connect polysilicon and metal



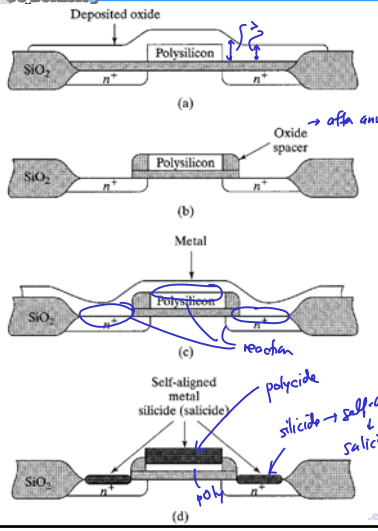
Silicide

- Sheet resistance of polysilicon and shallow diffusions used in CMOS are generally on the order of 10-20Ω/□
- Can reduce this resistance to 15-50 μΩ/□ by reacting silicon with a noble or refractory metal to form a silicide

TABLE 7.2 Properties of Some Silicides of Interest. Reprinted with permission of the American Institute of Physics from Ref [4].

Silicide	Starting Form	Sintering Temperature (°C)	Lowest Binary Eutectic Temperature (°C)	Specific Resistivity (μohm-cm)
$CoSi_2$	Metal on polysilicon	900	1195	18–25
	Cosputtered alloy	900		
$HfSi_2$	Metal on polysilicon	900	1300	45–50
$MoSi_2$	Cosputtered alloy	1000	1410	100
$NiSi_2$	Metal on polysilicon	900	966	50
	Cosputtered alloy	900		50–60
Pd_2Si	Metal on polysilicon	400	720	30–50
PtSi	Metal on polysilicon	600–800	830	28–35
$TaSi_2$	Metal on polysilicon	1000	1385	35–45
	Cosputtered alloy	1000		50–55
$TiSi_2$	Metal on polysilicon	900	1330	13–16
	Cosputtered alloy	900		25
WSi_2	Cosputtered alloy	1000	1440	70
$ZrSi_2$	Metal on polysilicon	900	1355	35–40

The Silicidation Process



- Expose silicon areas where silicidation is desired
- Blanket deposit metal
- Heat to needed temperature; can be done via rapid thermal anneal (RTA)
- Remove unreacted metal

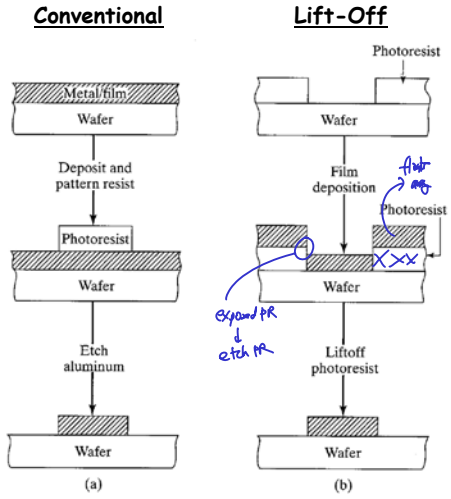
The Silicidation Process

Remarks:

1. Often can be self aligned to the region to be silicided, in which case it's called a salicide
2. Polycide: a silicide over polysilicon
   - Also pretty much self-aligned
   - Just put the metal down everywhere, heat, and reaction will only occur over polysilicon areas
3. Achieve resistivities from 15-50 μΩ-cm
4. Can oxidize the surface of a silicide, since silicon diffuses through the silicide to combine with the oxidant
5. Unlike silicon-metals that are unreacted, many silicides can take temperatures much higher than the eutectic temperature, over 1000°C
   - not true for all silicides, e.g., nickel silicide (900°C), platinum silicide (800°C), and palladium silicide (700°C)

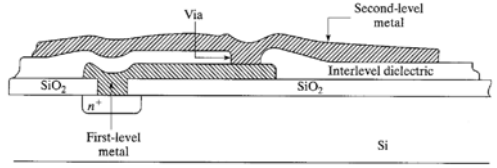
Lift-Off

- Many metals (e.g., nickel, copper) do not have a recipe for dry etching, so cannot be etched anisotropically with good resolution
- Lift-off provides a method for patterning a metal without the need for etching
- Right: comparison of conventional and lift-off based metallization processes

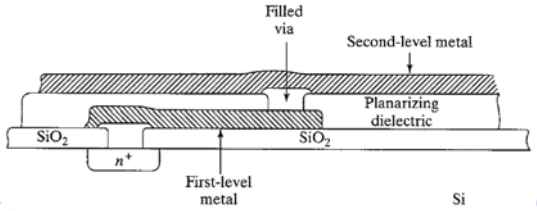


Multilevel Metallization

- Big Problem (for multi-levels of metal): topography
  - Interferes with lithography, degrading resolution
  - Creates stringers that then force overetching

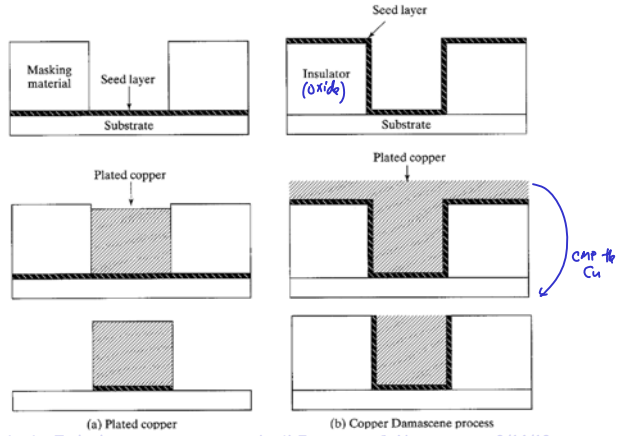


- Solution: planarization and contact plugs



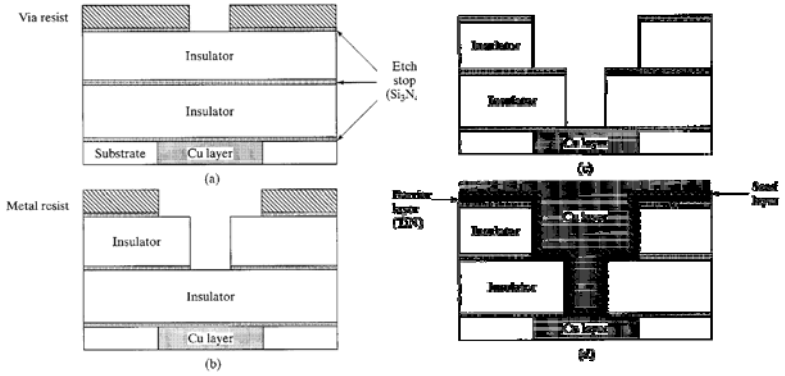
Damescene Process

- Employs plating through molds to achieve contact plugs in a fully-planarized (via CMP) cross-section



Dual Damescene Process

- Do multiple steps in one step
- Form interconnect lines and vias between interconnect levels all at the same time



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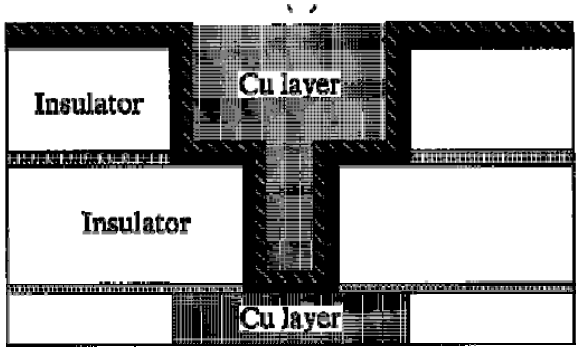
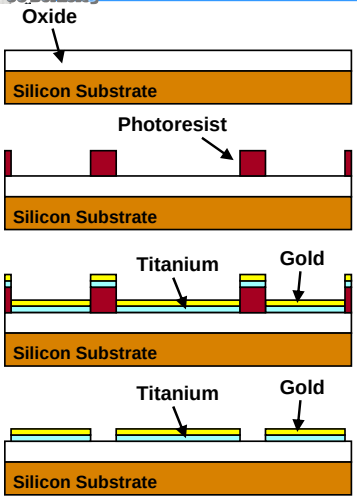


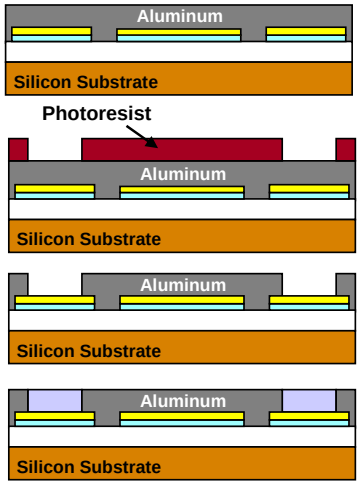
Nickel Surface-Micromachining Process Flow

Nickel Metal Surface-Micromachining



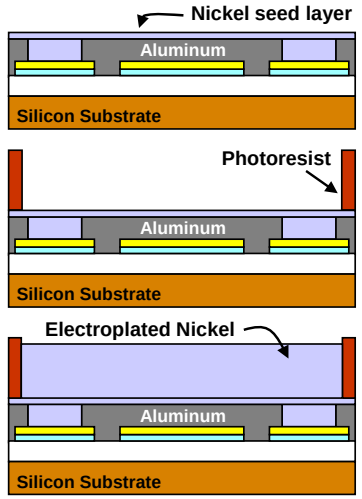
- Deposit isolation LTO:
  - Target = 2μm
  - 1 hr. 40 min. LPCVD @450°C
- Densify the LTO
  - Anneal @950°C for 30 min.
- Define metal interconnect via lift-off
  - Spin photoresist and pattern lithographically to open areas where interconnect will stay
  - Evaporate a Ti/Au layer
    - Target = 30nm Ti
    - Target = 270nm Au
  - Remove photoresist in PRS2000→ Ti/Au atop the photoresist also removed

Nickel Metal Surface-Micromachining



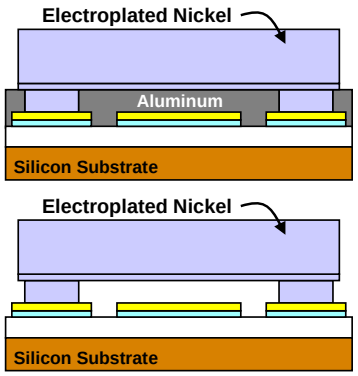
- Evaporate Al to serve as a sacrificial layer
  - Target = 1μm
- Lithography to define anchor openings
- Wet etch the aluminum to form anchor vias
  - Use solution of $H_3PO_4/HNO_3/H_2O$
- Remove photoresist in PRS2000
- Electroplate nickel to fill the anchor vias
  - Use solution of nickel sulfamate @ 50°C
  - Time the electroplating to planarize the surface

Nickel Metal Surface-Micromachining



- Evaporate a thin film of nickel to serve as a seed layer for subsequent Ni electroplating
  - Target = 20nm
- Form a photoresist mold for subsequent electroplating
  - Spin 6 um-thick AZ 9260 photoresist
  - Lithographically pattern the photoresist to delineate areas where nickel structures are to be formed
- Electroplate nickel structural material through the PR mold
  - Use a solution of nickel sulfamate @ 50°C
  - Cathode-to-anode current density ~ 2.5 mA/cm²

Nickel Metal Surface-Micromachining



- Strip the PR in PRS2000
- Remove the Ni seed layer in Ni wet etchant
- Release the structures
  - Use a $K_4Fe(CN)_6/NaOH$ etchant that attacks Al while leaving Ni and Au intact
  - Etch selectivity > 100:1 for Al:Ni and Al:Au

Nickel Surface-Micromachining Example

- Below: Surface-micromachined in nickel using the described process flow