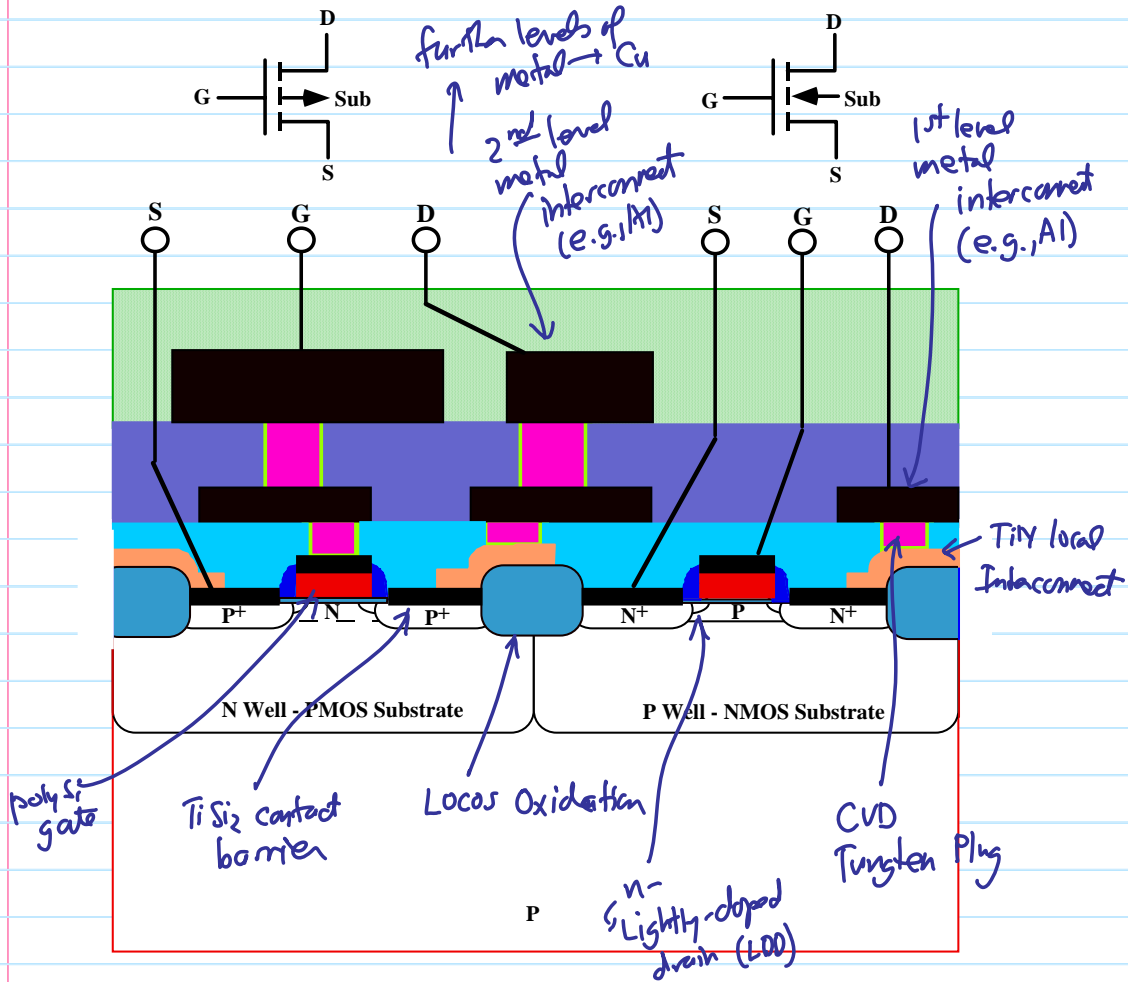


EE 143 CMOS Process Flow

CTN

1

Typical mid-2000's CMOS Process (good down to  $\sim 0.25\mu\text{m}$ )



Comments:

- ① Above cross-section uses LOCOS oxidation for device isolation  $\rightarrow$  this limits it to  $\sim 0.25\mu\text{m}$  processes  $\Rightarrow$  need trench isolation for smaller channel lengths
- ② TiSi<sub>2</sub> contact barriers over S/D junctions prevent metal spiking into the junctions.
- ③ Lightly doped drain (LDD) junctions reduce  $E$  fields that if too large generate "hot e-'s" that can degrade device performance  $\rightarrow$  a reliability problem.  
 $\hookrightarrow$  also help to reduce punchthrough

EE 143

CMOS Process Flow

CTN

2

*PR (photoresist)*

Photoresist  
Si<sub>3</sub>N<sub>4</sub>  
SiO<sub>2</sub>

SiO<sub>2</sub> Si<sub>3</sub>N<sub>4</sub>

Si, (100), P Type, 5-50  $\mu$ m

- Substrate selection: moderately high resistivity, (100) orientation, P type.
- Wafer cleaning, thermal oxidation ( $\approx 40$  nm), nitride LPCVD deposition ( $\approx 80$  nm), photoresist spinning and baking ( $\approx 0.5 - 1.0$   $\mu$ m).

P

- Mask #1 patterns the active areas. The nitride is dry etched.

Field Oxide

*nitride bends up during LOCOS oxidation*

Bird's Beak

- Field oxide is grown using a LOCOS process. Typically 90 min @ 1000°C in H<sub>2</sub>O grows  $\approx 0.5$   $\mu$ m.

*encroaches on the device (shallow trench isolation is a better approach!)*

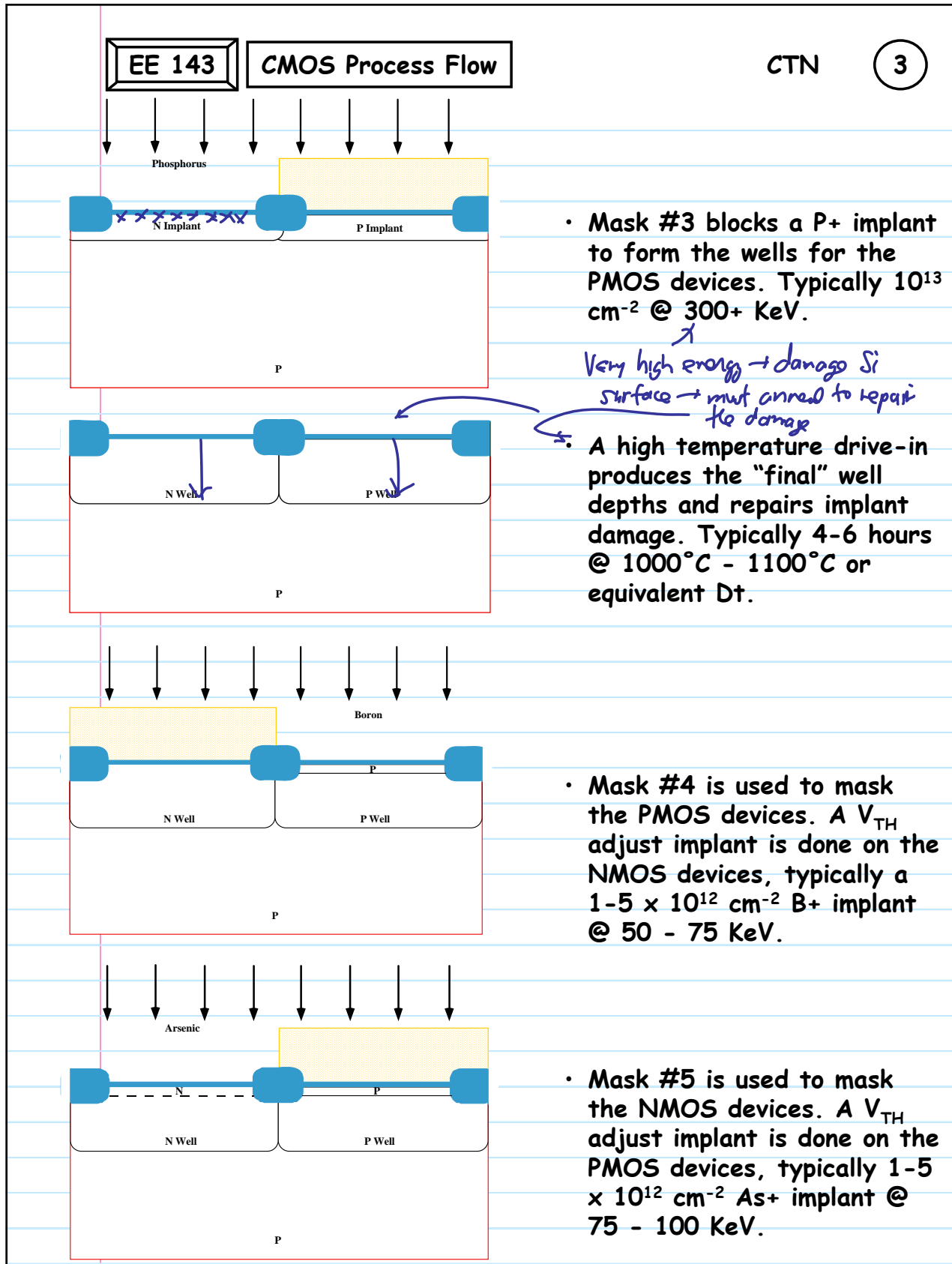
Boron

P Implant

*single implant realizes both the well & the channel stop layer*

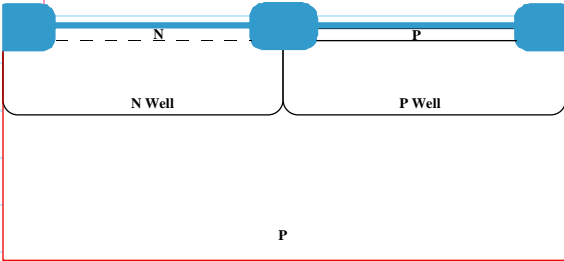
*implant through the field oxide & not easy to do, but saves money*

P

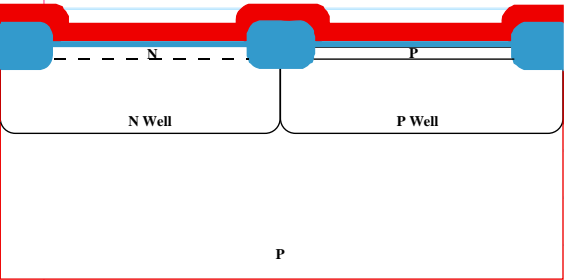


EE 143 CMOS Process Flow

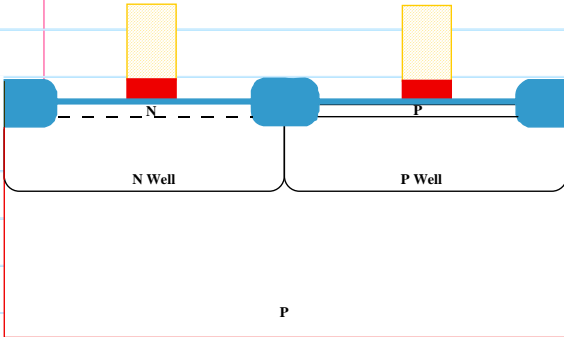
CTN 4



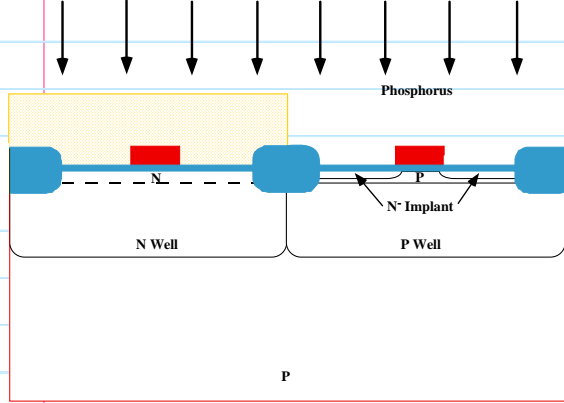
- The thin oxide over the active regions is stripped and a new gate oxide grown, typically 3 - 5 nm, which could be grown in 0.5 - 1 hrs @ 800 °C in O<sub>2</sub>.



- Polysilicon is deposited by LPCVD ( $\approx 0.5 \mu\text{m}$ ). ~~An unmasked P+ or As+ implant dopes the poly (typically  $5 \times 10^{15} \text{cm}^{-2}$ ).~~



- Mask #6 is used to protect the MOS gates. The poly is plasma etched using an anisotropic etch.



- Mask #7 protects the PMOS devices. A P+ implant forms the LDD regions in the NMOS devices (typically  $5 \times 10^{13} \text{cm}^{-2}$  @ 50 KeV).

*This is done because the previous oxide is damaged after numerous implants.*