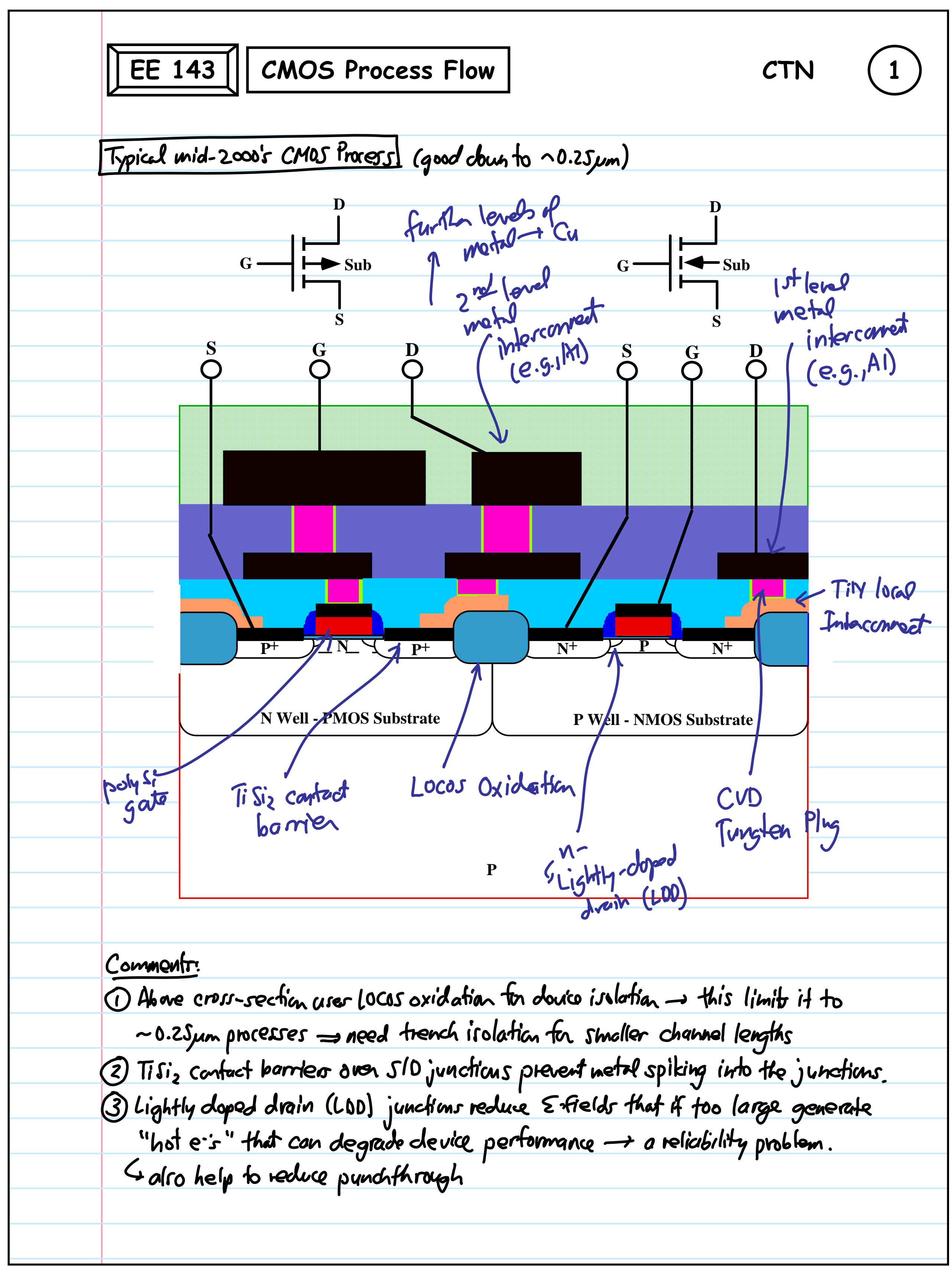

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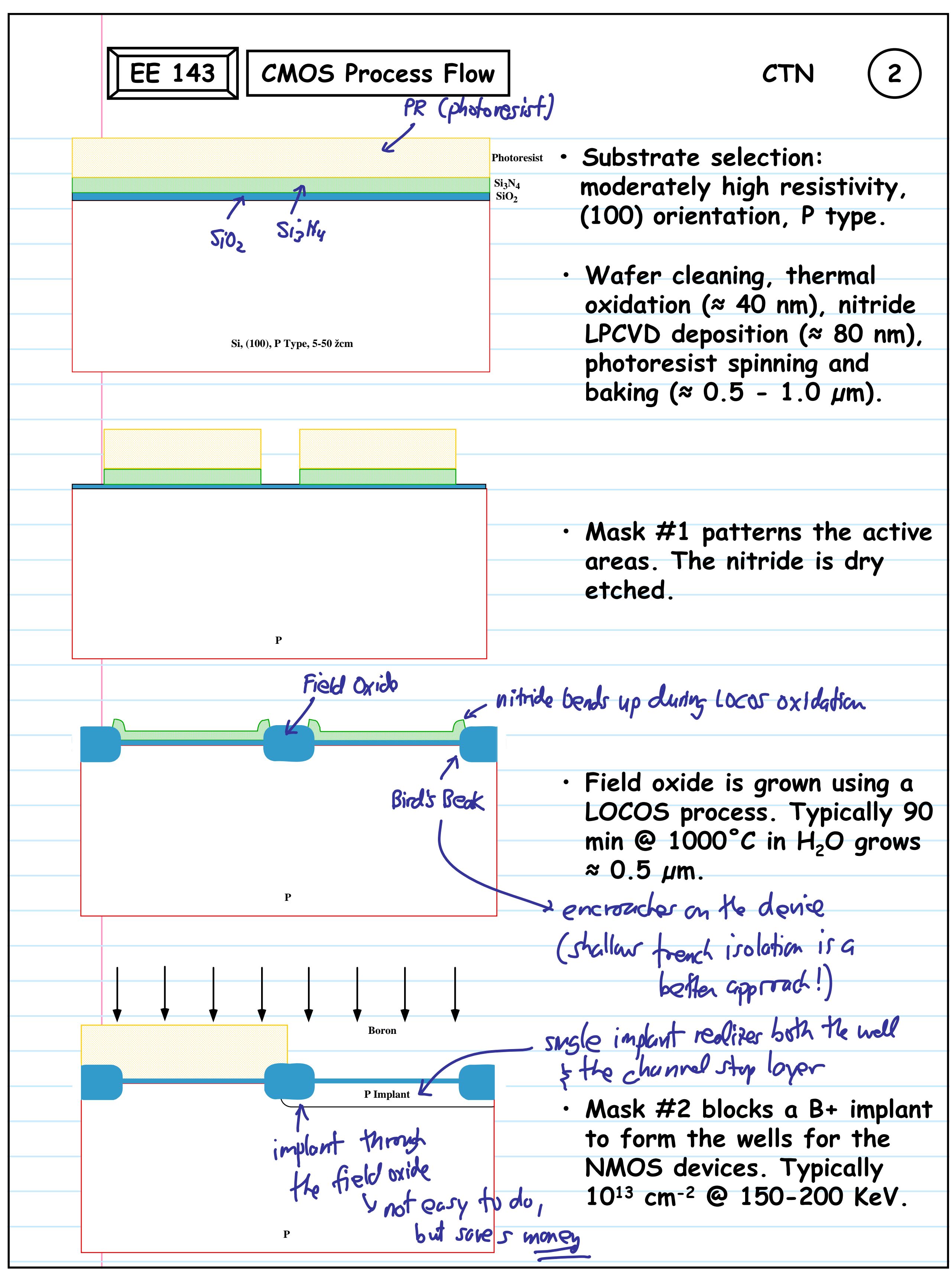

- Substrate selection: moderately high resistivity, (100) orientation, P type.
- Wafer cleaning, thermal oxidation (≈ 40 nm), nitride LPCVD deposition (≈ 80 nm), photoresist spinning and baking (≈ 0.5 - 1.0 μm).
- Mask #1 patterns the active areas. The nitride is dry etched.
- Field oxide is grown using a LOCOS process. Typically 90 min @ 1000°C in H_2O grows ≈ 0.5 μm.
- Mask #2 blocks a B+ implant to form the wells for the NMOS devices. Typically 10^{13} cm^{-2} @ 150-200 KeV.

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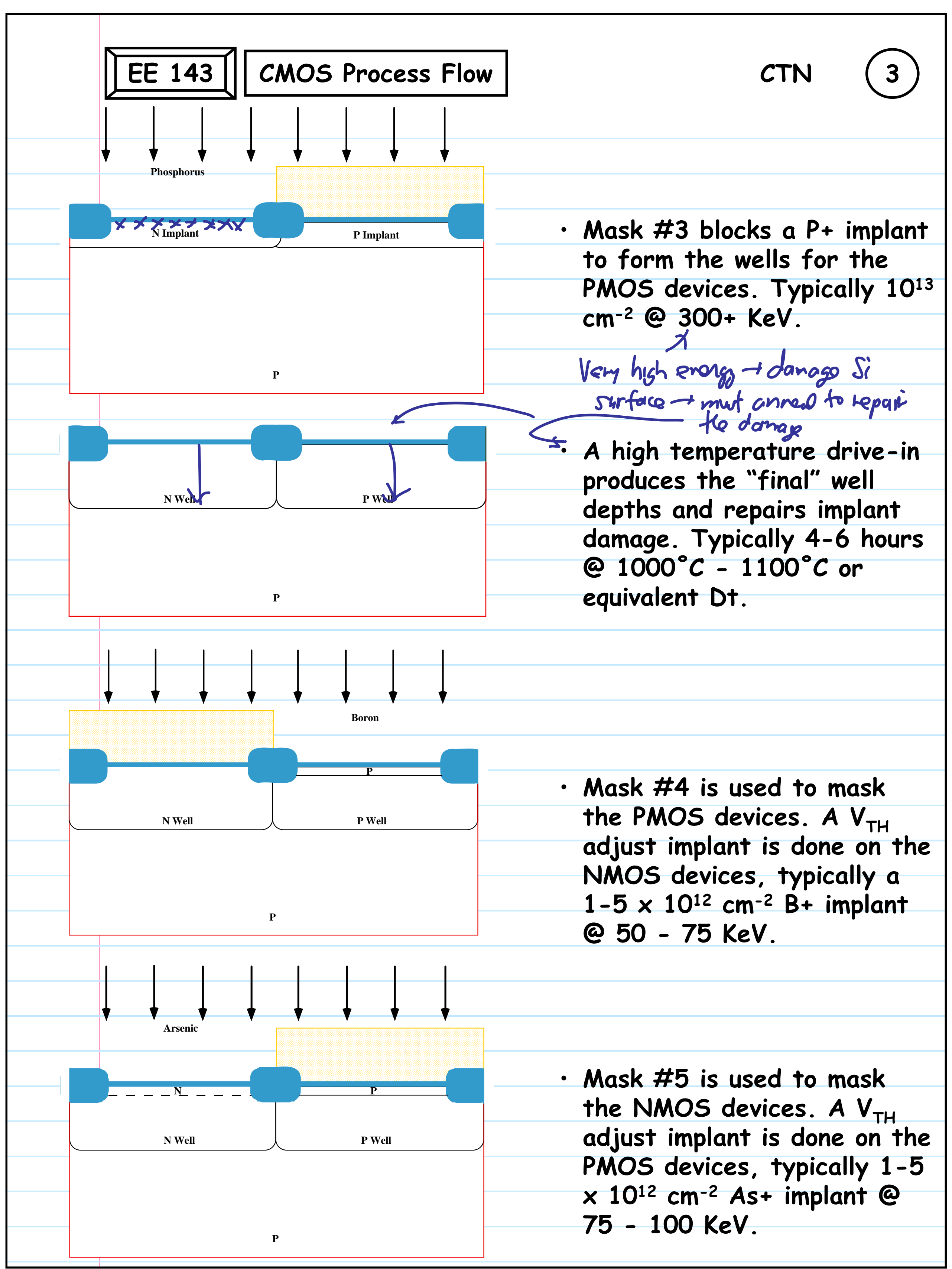

- Mask #3 blocks a P+ implant to form the wells for the PMOS devices. Typically 10^{13} cm^{-2} @ 300+ KeV.
- A high temperature drive-in produces the “final” well depths and repairs implant damage. Typically 4-6 hours @ 1000°C - 1100°C or equivalent Dt.
- Mask #4 is used to mask the PMOS devices. A V_{TH} adjust implant is done on the NMOS devices, typically a 1-5 x 10^{12} cm^{-2} B+ implant @ 50 - 75 KeV.
- Mask #5 is used to mask the NMOS devices. A V_{TH} adjust implant is done on the PMOS devices, typically 1-5 x 10^{12} cm^{-2} As+ implant @ 75 - 100 KeV.

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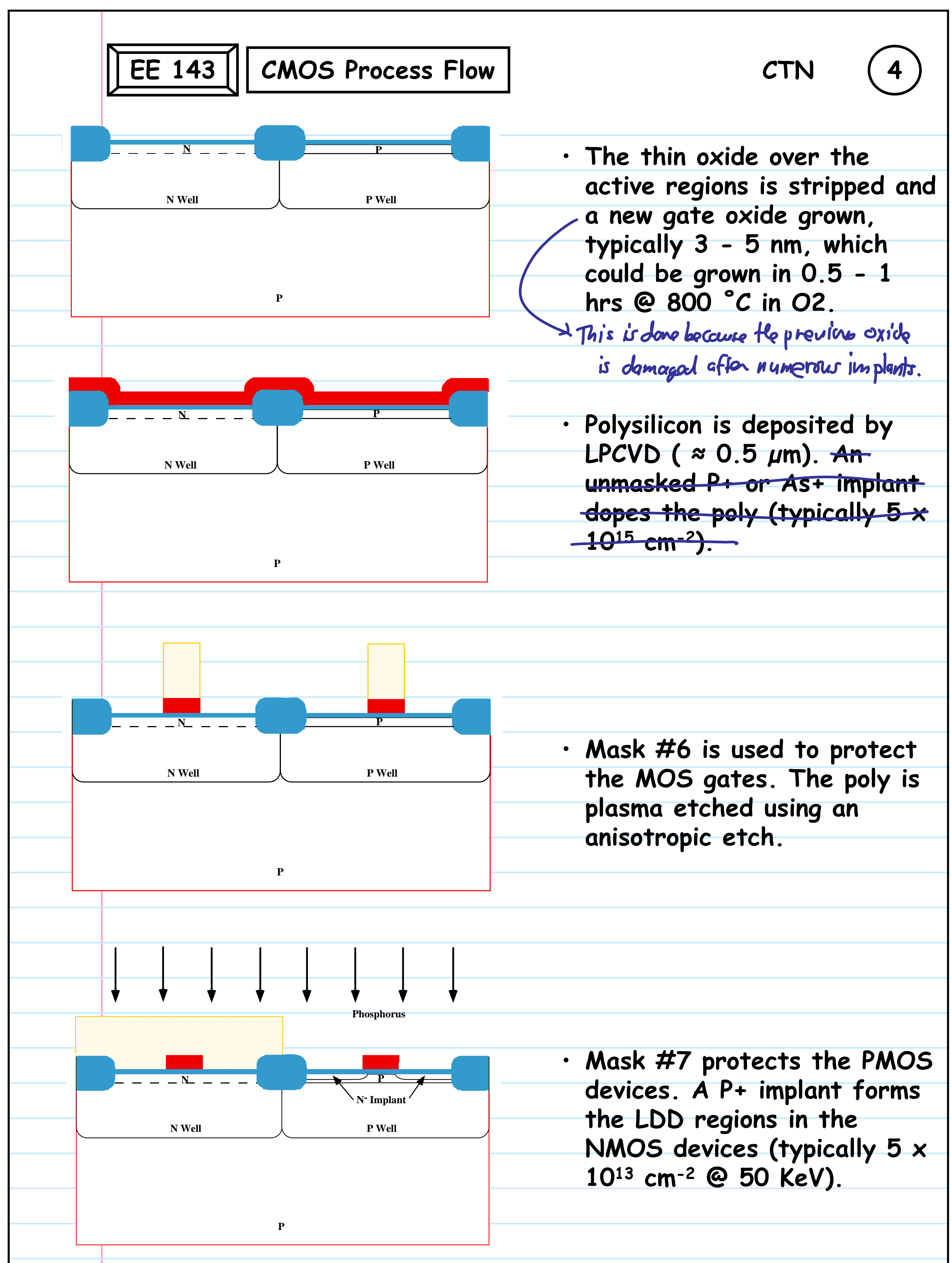

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