Lecture 22: Advanced CMOS & Punchthrough

- Announcements:
- Lab 1 Report will due Friday, April 23
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- Lecture Topics:
  - Advanced CMOS
  - Punchthrough
  - Isolation
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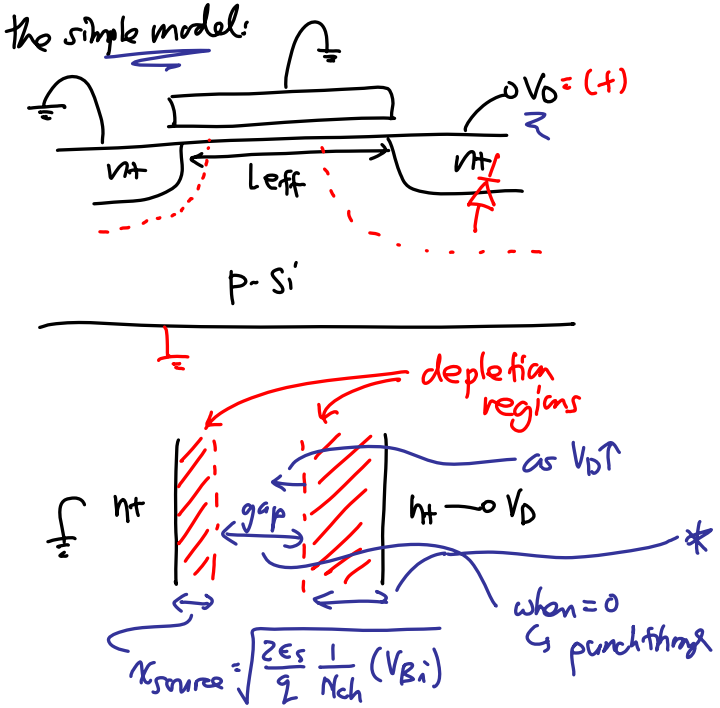
- Last Time:
- Going through Advanced CMOS notes … continue with this to start today

Punchthrough

⇒ the simple model:



ϵ_s: permittivity in Si ($\epsilon_r = 11.7$)

N_{ch}: substrate doping near the channel

V_{Bi}: built-in potential

$$= \frac{kT}{q}\ln\left[\frac{N_D(n+)}{n_i}\right] + \frac{kT}{q}\ln\left[\frac{N_A}{n_i}\right] \leftarrow N_{ch}$$

↑ 0.56 V

$$* \rightarrow x_{drain} = \sqrt{\frac{2\epsilon_s}{q}\frac{1}{N_{ch}}(V_{Bi} + V_D)}$$

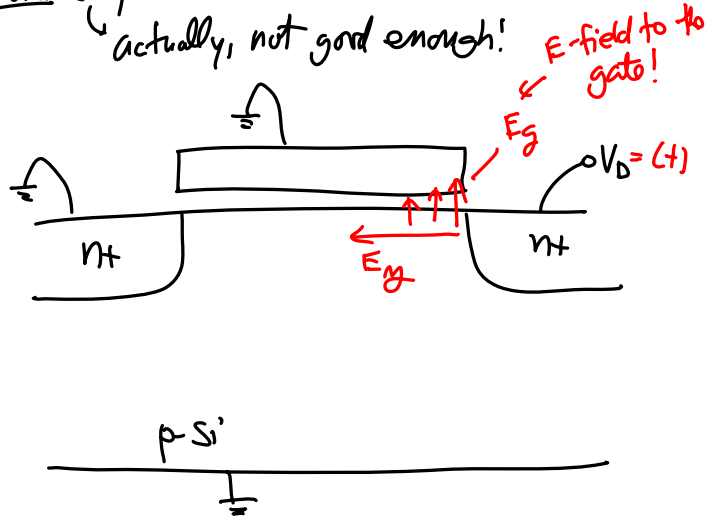
When gap → 0 ⇒ punchthrough → current can flow!

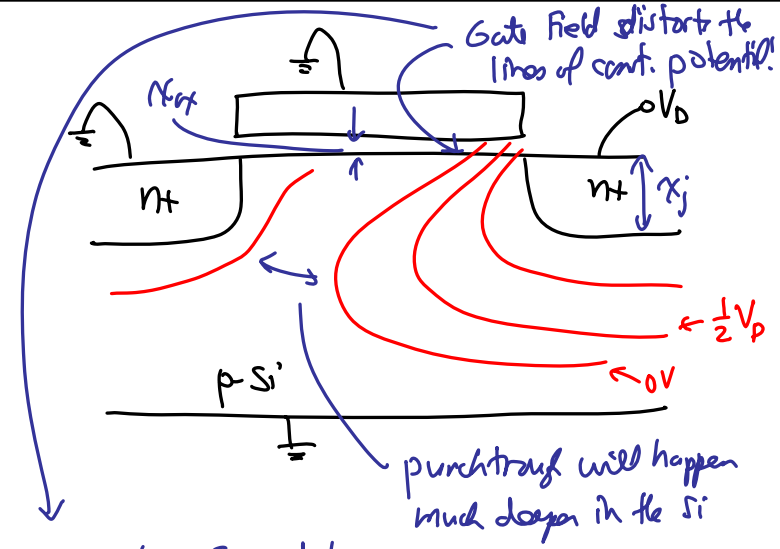
↳ when $x_{source} + x_{drain} \geq L_{eff}$ ⊃ punchthrough!

↳ get leakage current (can't turn the device off!)

Above: simple model

↳ actually, not good enough!





as $x_{ox}\downarrow \rightarrow$ E_g gets larger!
↳ punchthrough is suppressed close to the surface!
if $x_j\downarrow$ $\rightarrow$ ∴ less punchthrough leakage I_D!

Thus, bulk punchthrough depends on:

	$L\downarrow$	$x_j\downarrow$	$x_{ox}\downarrow$	$N_{ch}\uparrow$
punch-through	worse	better	better	better

Go back to the Advanced CMOS lecture notes.

… then go to the Isolation lecture notes.