Lecture 25: V_t Implant

- Announcements:
- Lab 1 Report previously due Friday, April 23 – change to Monday, April 26, 7 p.m.
- Lab 2 Report will be due Friday, May 7 (during the RRR week), 7 p.m.
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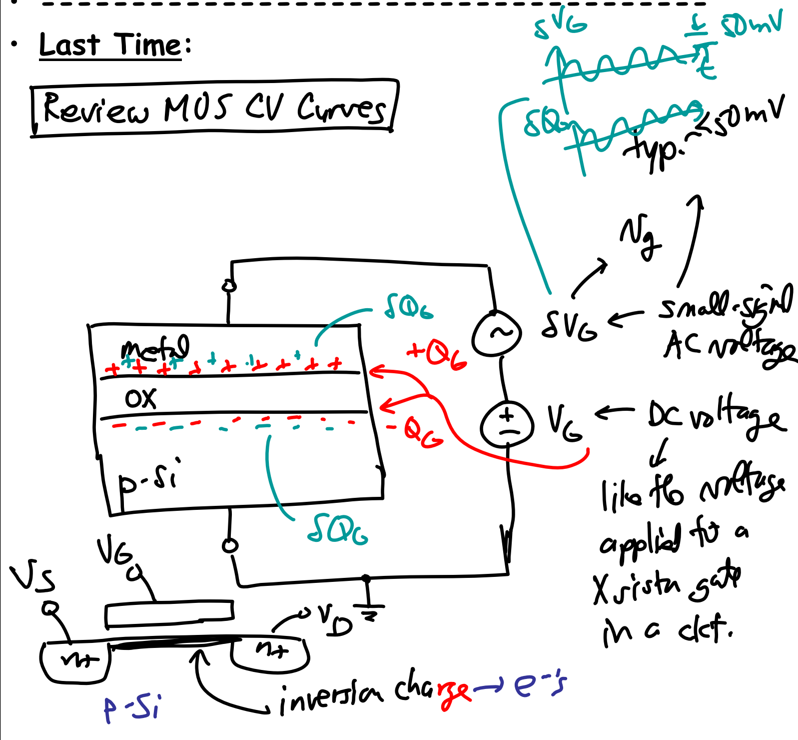
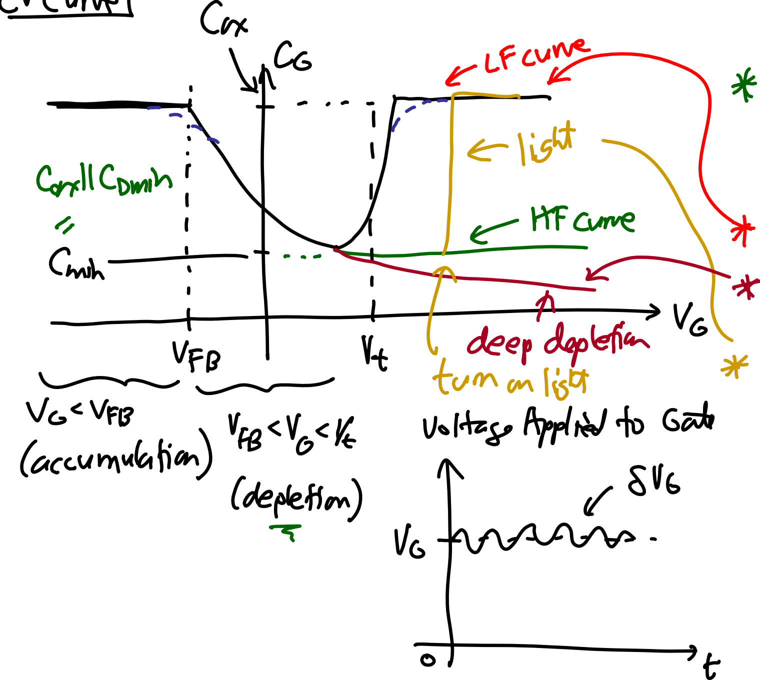
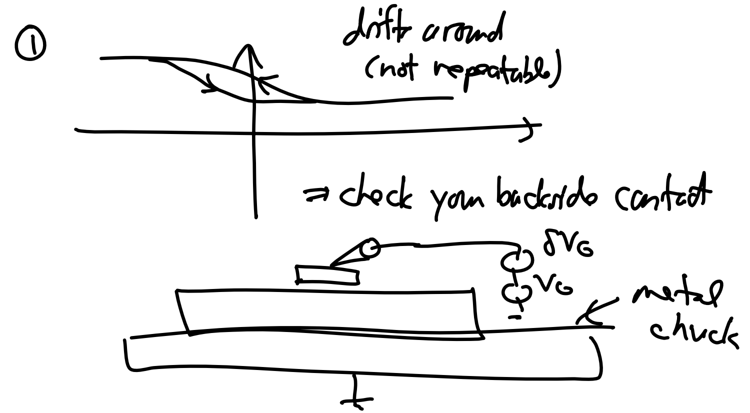
- Lecture Topics:
  - MOS CV problems & solutions
  - Threshold Implant
    - Threshold voltage
    - Needed ΔV_t
    - V_t Implant Cases
- --
- Last Time:







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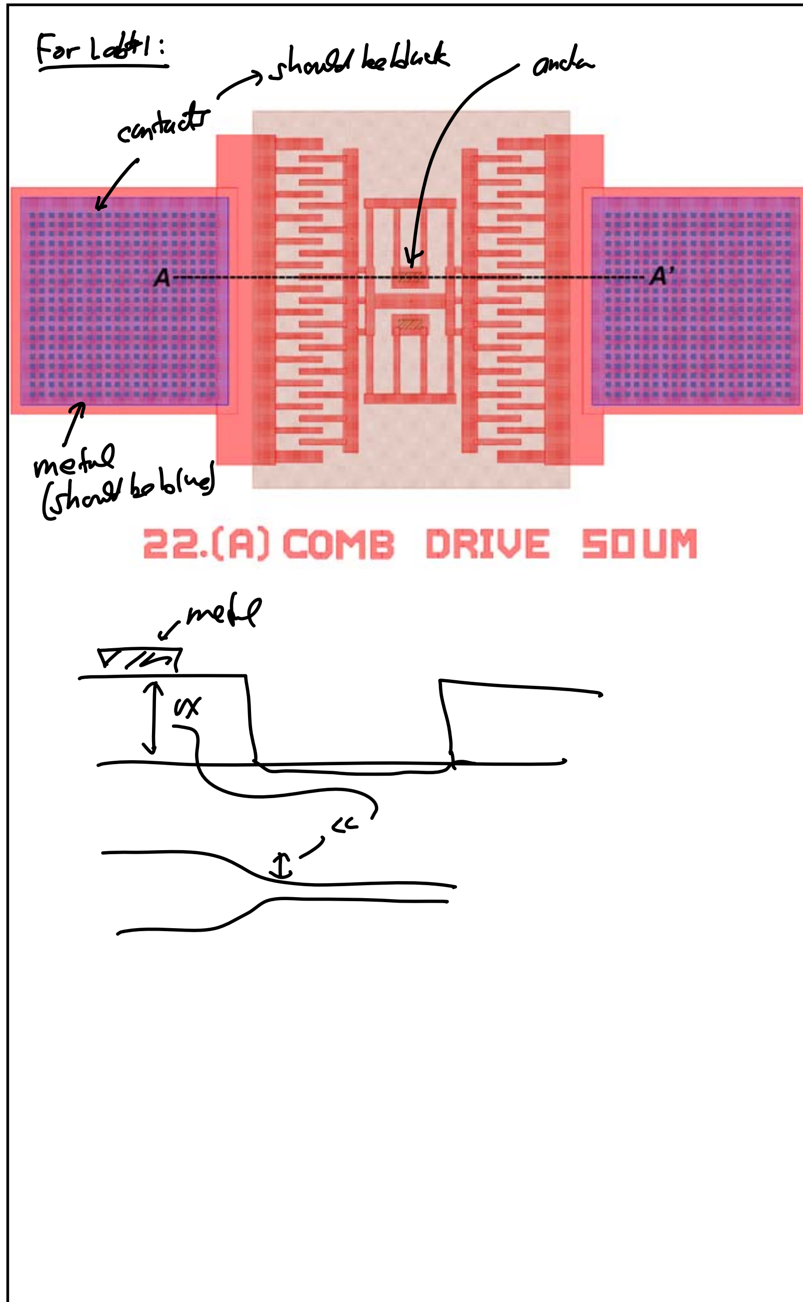

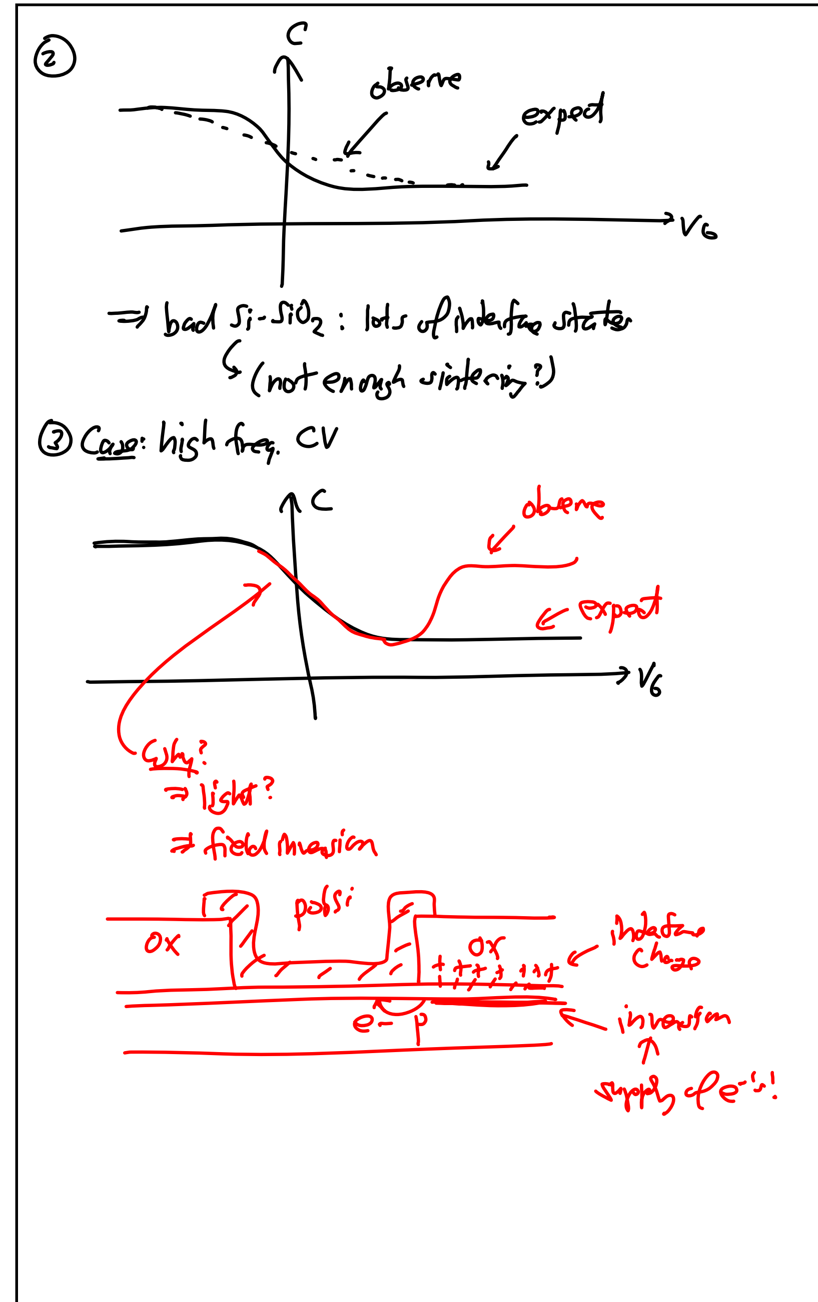

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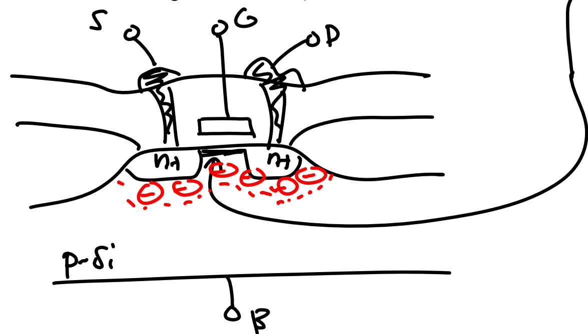
Threshold Implant

⇒ implant to tailor/adjust the threshold voltage V_t of an MOS device

Def.: Threshold Voltage: gate voltage V_{GS} ($= V_G - V_S$) required to produce an inversion layer



Question: How is V_t best adjusted? What factors most impact V_t?

$$V_t = \phi_{ms} - \psi_s - \frac{Q_{ss}}{C_{ox}} - \frac{Q_B}{C_{ox}}$$

, where

ϕ_{ms} = work function difference [in V] between gate material and bulk Si (same as V_{FB})

ψ_s = surface potential in Si @ onset of strong inversion
$= 2\phi_f$ for uniformly doped substrate ($|\phi_f| \sim 0.3V$)

Q_{ss} = oxide charge per unit area @ the oxide-Si interface [C/cm^2]

Q_B = charge stored in the depletion region (at the onset of inversion)

$$|Q_B| = \sqrt{2q\epsilon_s N_B (2|\phi_f| + |V_{SB}|)} \quad [C/cm^2]$$

N_B: conc. in bulk; V_{SB}: reverse bias

$$x_{dmax} = \sqrt{\frac{2\epsilon_s}{q}\frac{1}{N_B}(2|\phi_f| + |V_{SB}|)}$$

C_{ox} = gate oxide capacitance per unit area [F/cm^2]

Case: $V_{SB}=0$

$$V_t(V_{SB}=0) = V_{to} = \phi_{ms} - 2\phi_f - \frac{Q_{ss}}{C_{ox}} - \frac{Q_{BO}}{C_{ox}}$$

$$|Q_{BO}| = \sqrt{2q\epsilon_s N_B (2|\phi_f|)}$$

Then:

$$V_t = \phi_{ms} - 2\phi_f - \frac{Q_{ss}}{C_{ox}} - \frac{Q_B}{C_{ox}}$$

$$= \underbrace{\phi_{ms} - 2\phi_f - \frac{Q_{ss}}{C_{ox}} - \frac{Q_{BO}}{C_{ox}}}_{V_{to}} - \frac{Q_B - Q_{BO}}{C_{ox}}$$

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$$V_t = V_{t0} - \gamma\left(\sqrt{2|\phi_F| + |V_{SB}|} - \sqrt{2|\phi_F|}\right)$$

$$\gamma = \frac{1}{C_{ox}}\sqrt{2q\epsilon_s N_B}$$

Signs in the V_t equation:

Parameter	NMOS	PMOS
Substrate	p-type	n-type
ϕ_{ms}:		
metal gate	−	−
n+ Si gate	−	−
p+ Si gate	+	+
ϕ_F	−	+
Q_{B0} (α Q_B)	−	+
Q_{ss}	+	+
γ	−	+
C_{ox}	+	+

Parameters to Adjust:

① $\psi_s = 2\phi_F$: $\phi_F = \frac{kT}{q}\ln\left(\frac{N_D}{n_i}\right)$ for n-substrate (← n-doping conc.)

$\phi_F = \frac{kT}{q}\ln\left(\frac{n_i}{N_A}\right)$ for p-substrate (← p-doping conc.)

intrinsic conc. ← for undoped Si

These are logarithmic w/ doping conc.!
i.e., 10X increase in $N_B \rightarrow 2.3\frac{kT}{q} \sim 60\text{mV}$ ← very small change

∴ ϕ_F not a good way to adjust V_t

② $\phi_{ms} = \phi_{F(sub)} - \phi_{F(gate)}$ → ineffective for the same reason as ↑

③ $|Q_B| = \sqrt{2q\epsilon_s N_B\left(2|\phi_F| + |V_{SB}|\right)}$ ← *

can increase $|Q_B|$ w/ $N_B\uparrow$
(can get significant ΔV_t here)

...but if you must increase N_B too much:
⇒ problems: ① lower carrier mobility, $\mu\downarrow$
② S/D capacitance ↑
③ lower junction breakdown voltage

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* → Can also $\Delta V_{SB} \rightarrow \Delta V_t$

↳ impractical → many devices would need to have their own well → too much area!

④ $C_{ox}\downarrow$ → but then low drive

⑤ $\frac{Q_{ss}}{C_{ox}}$: Q_{ss} due to oxide-Si interface charge

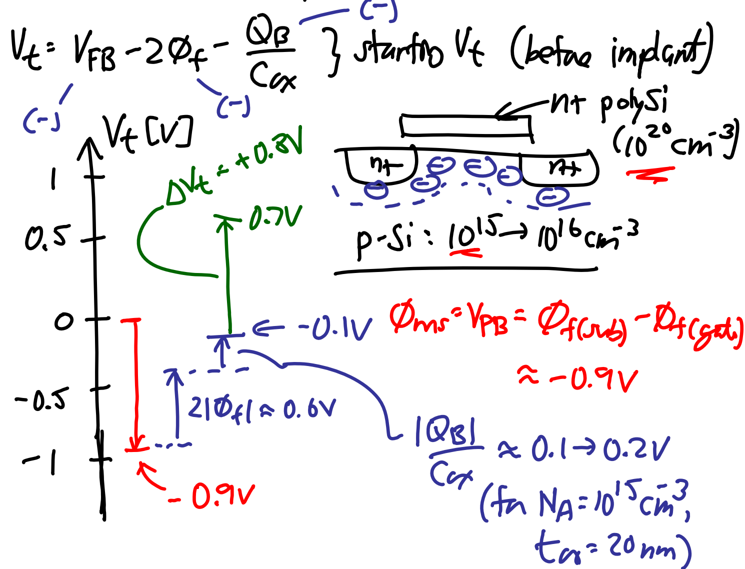
not controllable (easily)

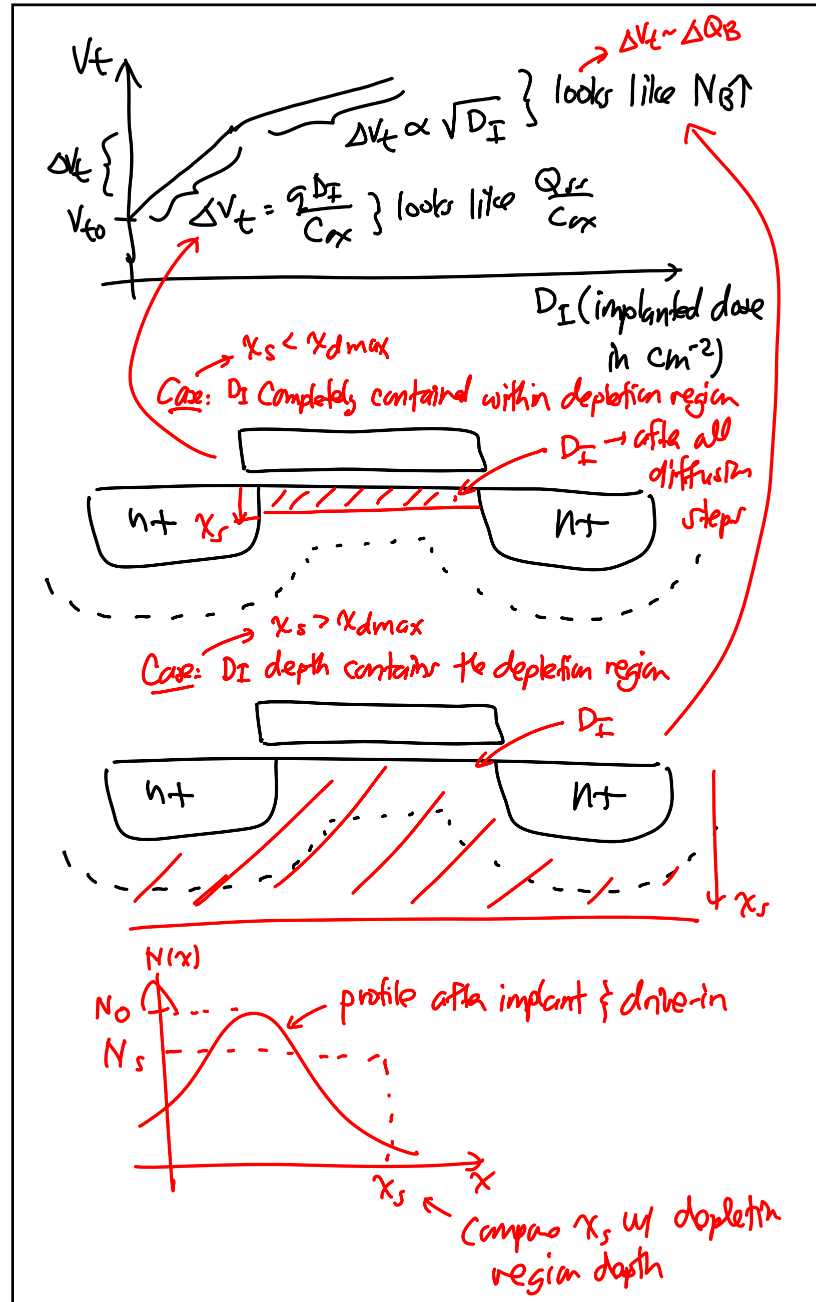
↑ want to minimize

↳ but if we could introduce a controlled amount of Q_{ss} → best way to set ΔV_t

Ex. Threshold Implant for NMOS

↳ enhancement implant





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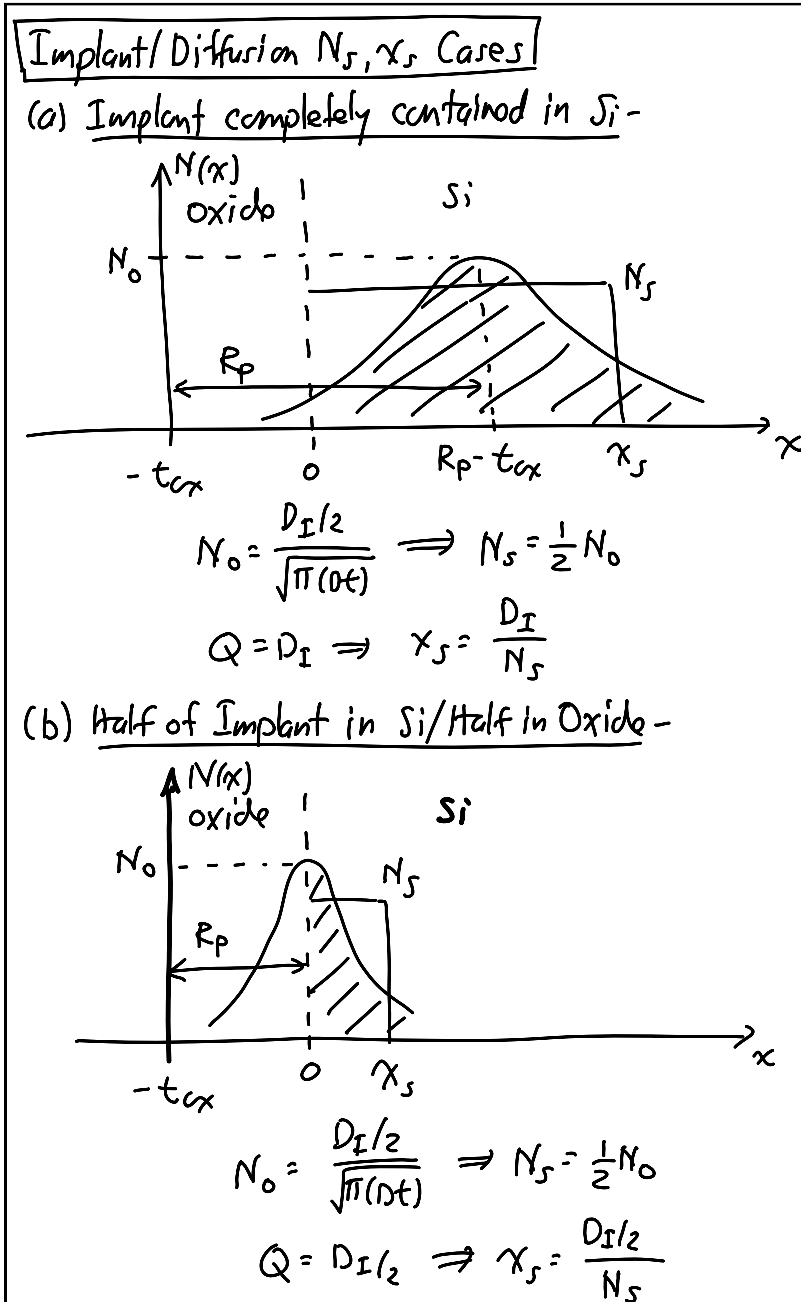

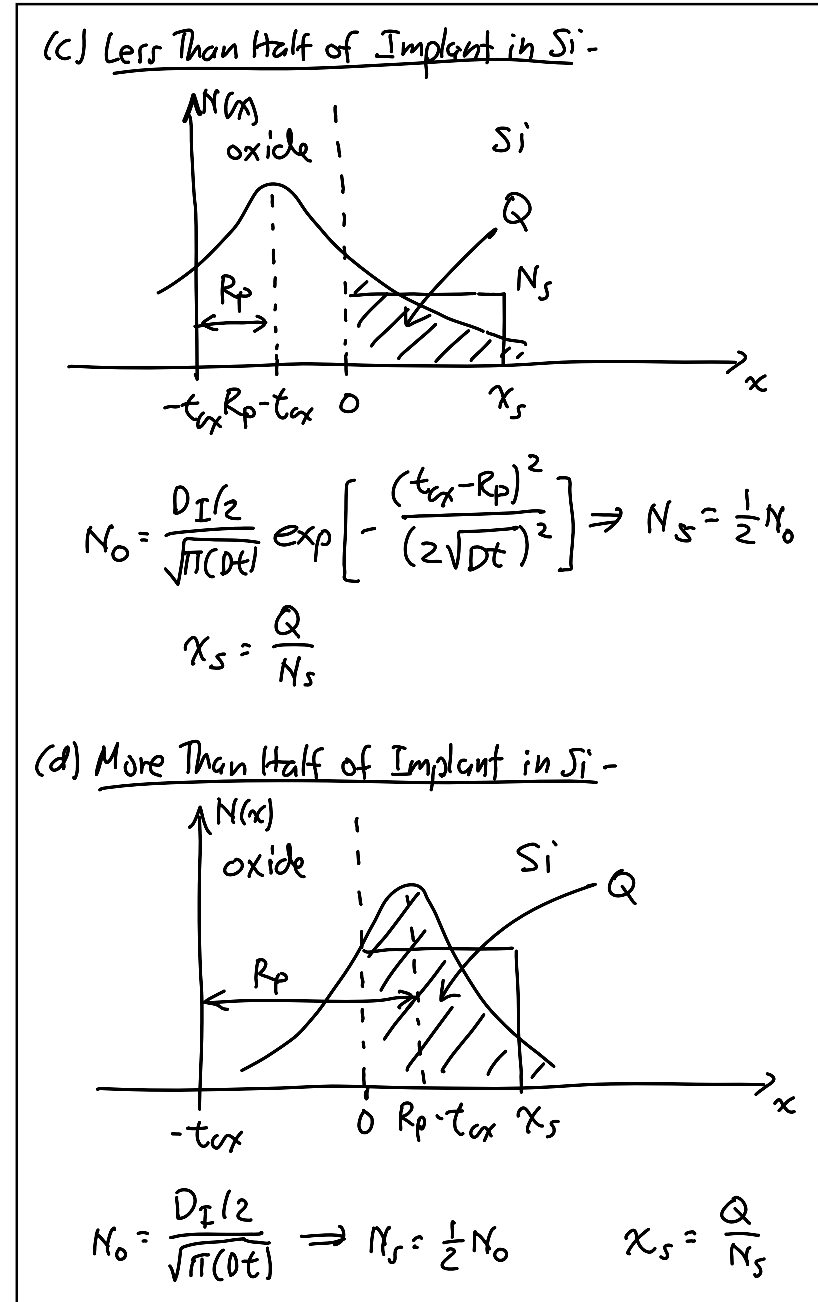

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