

- Diffusion:
- Process of introducing dopants into selected areas on an IC
- Example:

diborane gas \rightarrow $B_2H_6 + O_2$ @ high temperature $\sim 800^\circ C - 1200^\circ C$

SiO₂ B B B B B SiO₂

n-Si substrate

- ① Form borosilicate glass w/ high B concentration
- ② Boron diffuses in \rightarrow this becomes p-type

\Rightarrow diffusion requires:

- ① concentration gradient
- ② movement (velocity)

\Rightarrow Example. Fish Tank

- ① When separation removed...
- ② Fish will go to the other side
- ③ Until the concentration is the same on both sides

highly concentrated

But they can't if they're dead!

It's similar for an impurity in silicon:

need temperature for this to happen

Need high T for this vacancy to exist.

Just one mechanism for diffusion \rightarrow well look at other, too

Substitutional diffusion:

- \Rightarrow impurity moves along vacancy in the lattice
- \Rightarrow substitutes for a Si atom in the lattice

For movement to occur:

- ① Vacancies must exist.
- ② The B must have enough energy to move.

Both require high temperature!

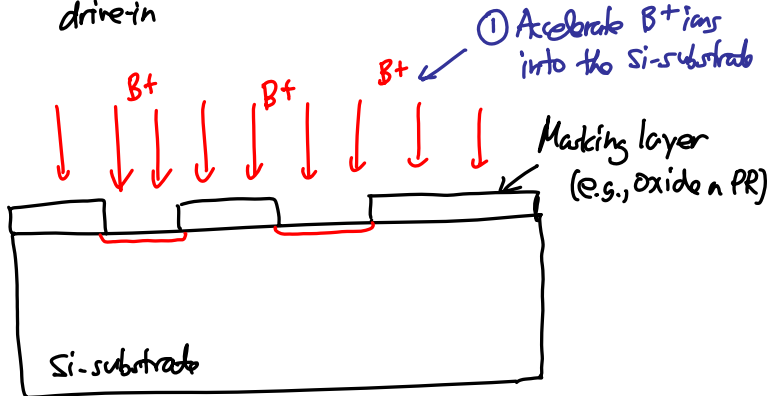
\rightarrow must heat to induce diffusion of impurities in Si!

Definitions:

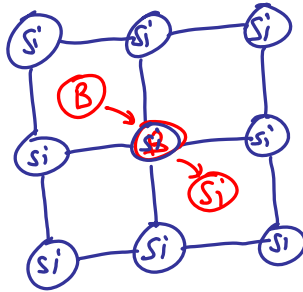
- ① Predeposition: diffusion w/ dopant source present
- ② Drive-in: diffusion in an inert ambient, e.g., N₂ w/ no dopant gases present

Ion Implantation

⇒ a more accurate way to introduce dopants before drive-in



② B⁺ punches into the Si



③ Raise T to move the B into the lattice → only when it's in the lattice is it active & can contribute to the doping level

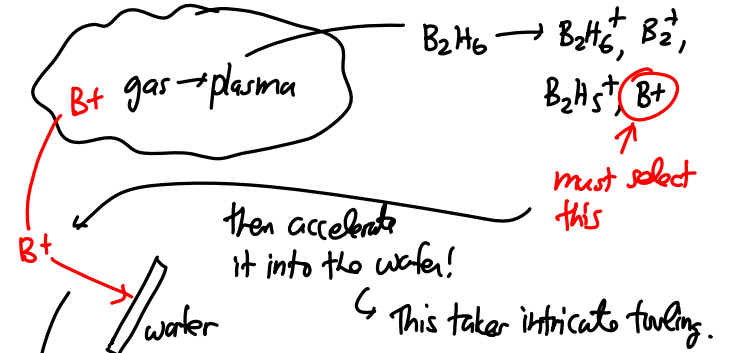
④ Keep T up to drive the dopants in to the desired depth.

Advantages:

- ① accurate dose
- ② change depth by setting ion energy
- ③ no need for high temperature

Problem: COST!

An ion implanter is quite a sophisticated piece of equipment! → and expensive! (> \$1 million)



Energy Range: 20keV - 100keV

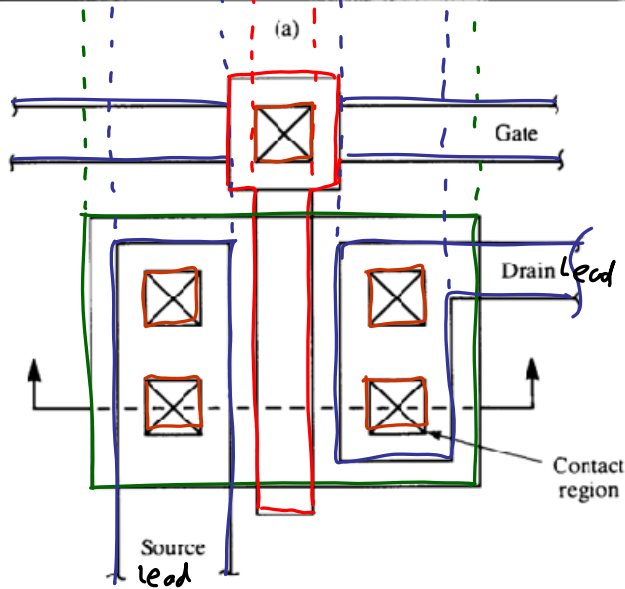
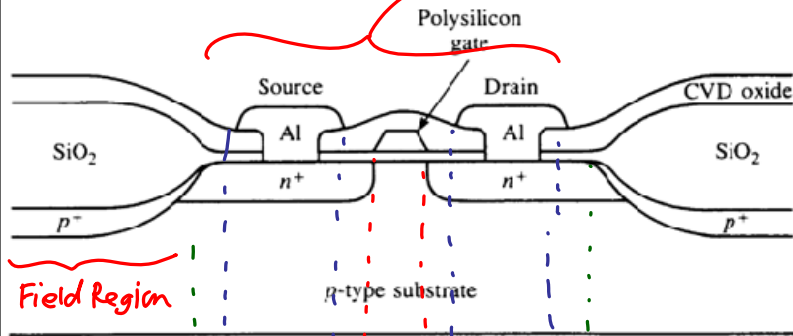
Penetration Depth: fraction of a μm

⇒ larger ions don't go as far as smaller

(heavier ions penetrate shallower than smaller.)

Dose: 10¹¹ - 10¹⁵ cm⁻²

- Process Integration:
- e.g., Standard NMOS Process
- Similar to EE143 process, but a bit more advanced
- Difference:
 - ↳ 5 masks (vs. 4 for EE143)
 - ↳ LOCOS oxidation (local oxidation) (oxidation and etch back for EE143)
- The Goal: NMOS device



5 Masks

Gate Poly-silicon Mask (cf)

Active Area Mask (cf)

Contact Mask (df)

Metal Mask (cf)

Bond Pad Opening Mask (df)

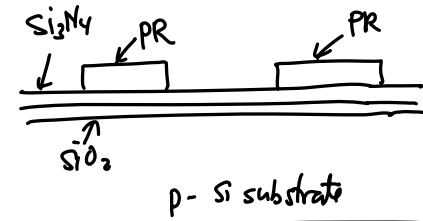
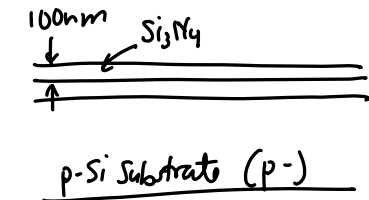
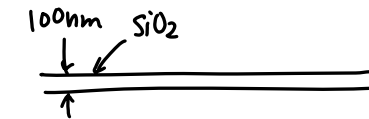
for (+) PR
 Clear field → box indicates region of PR that remain after lithography
 for (+) PR
 dark field → box indicates region of PR removed after lithography
 → not shown

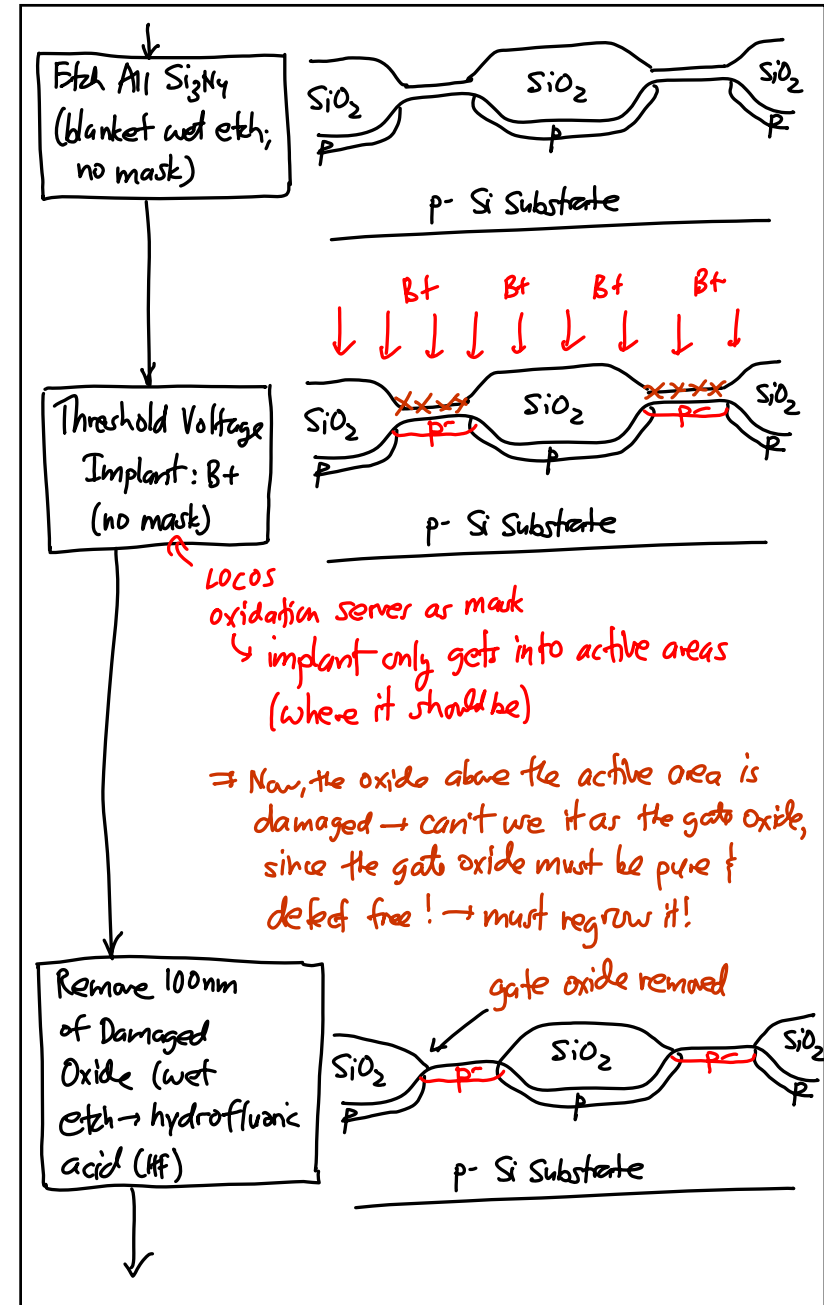
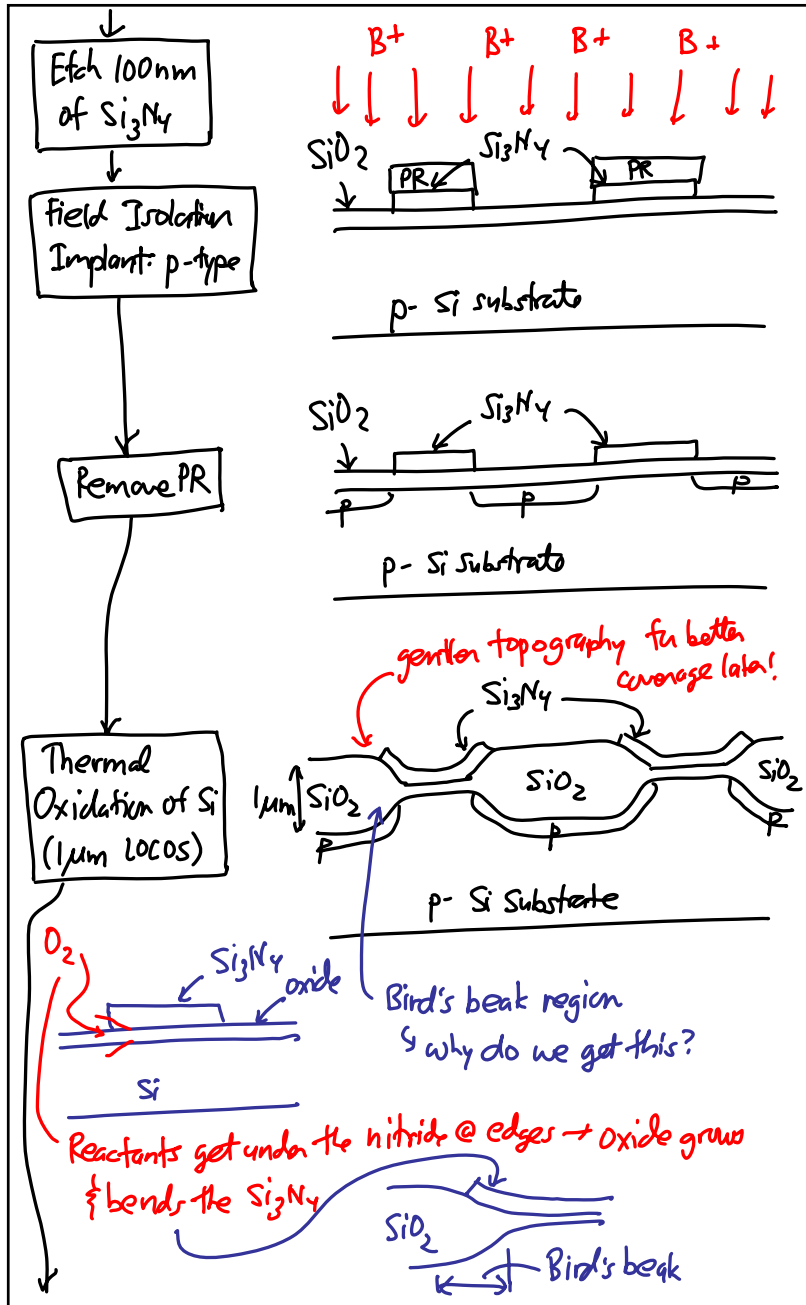
NMOS Process Flow

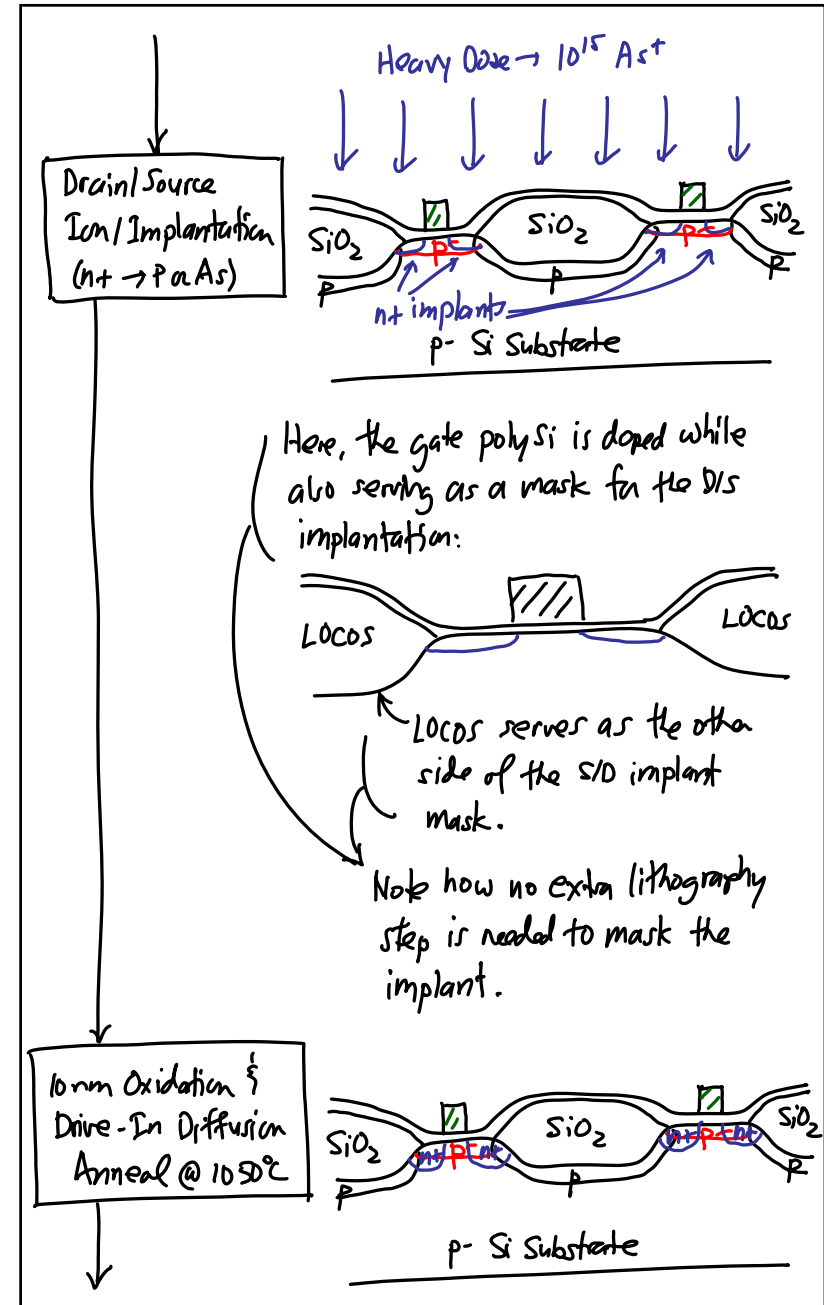
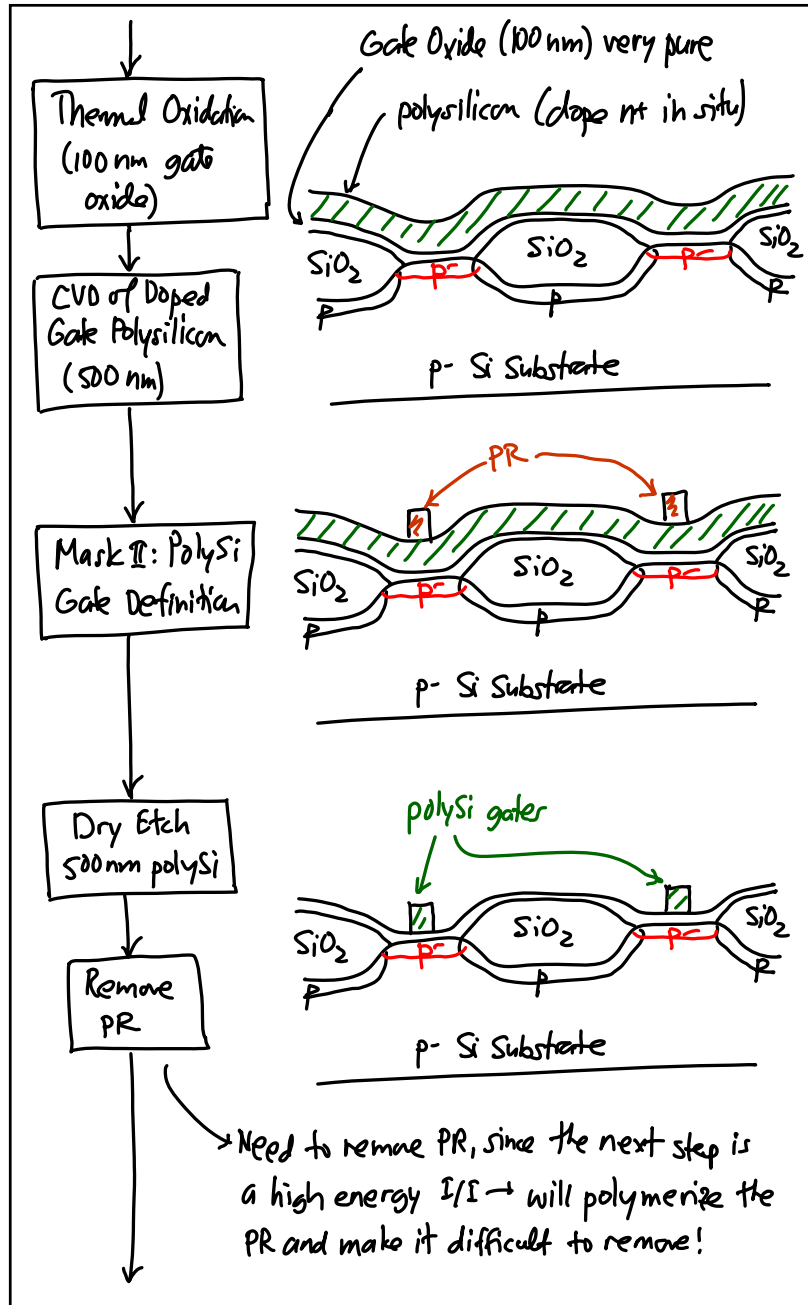
Silicon Oxidation thickness = 100nm

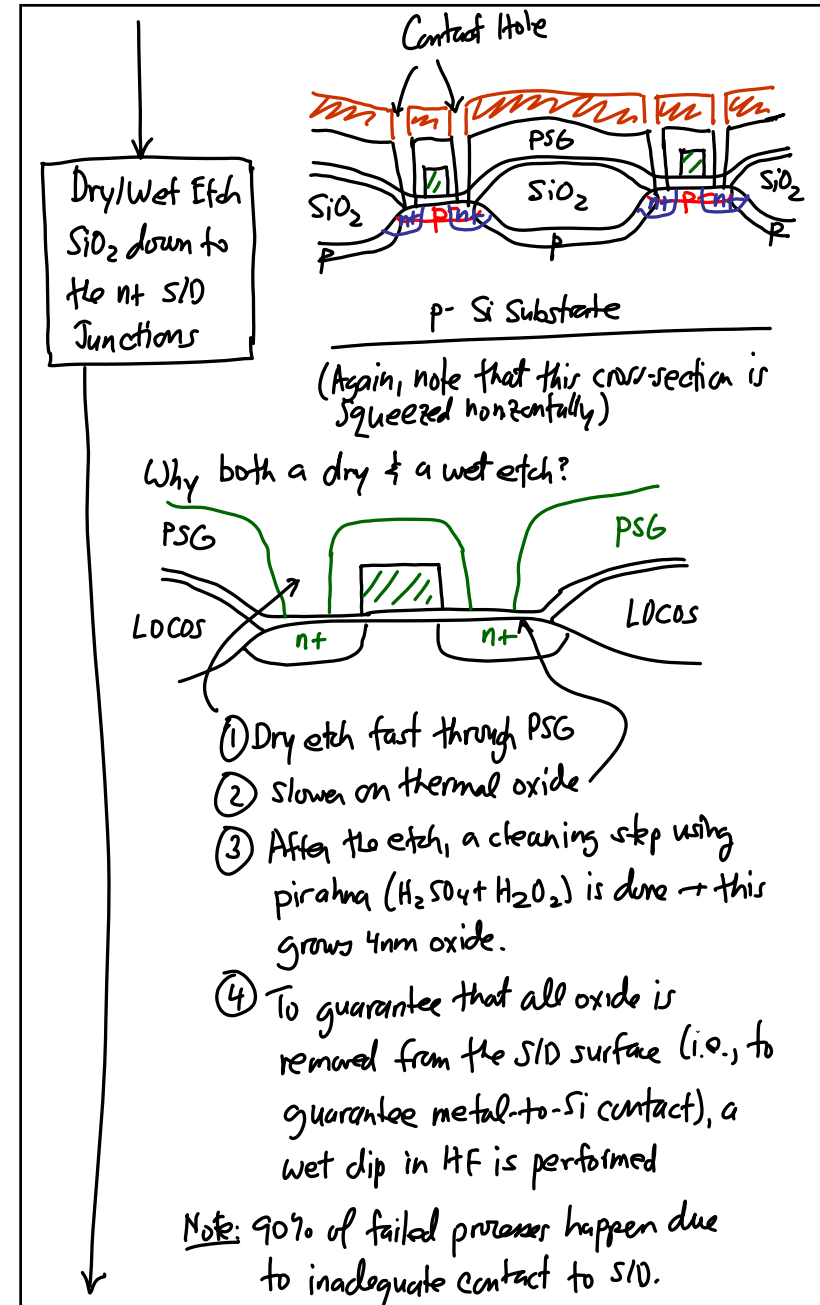
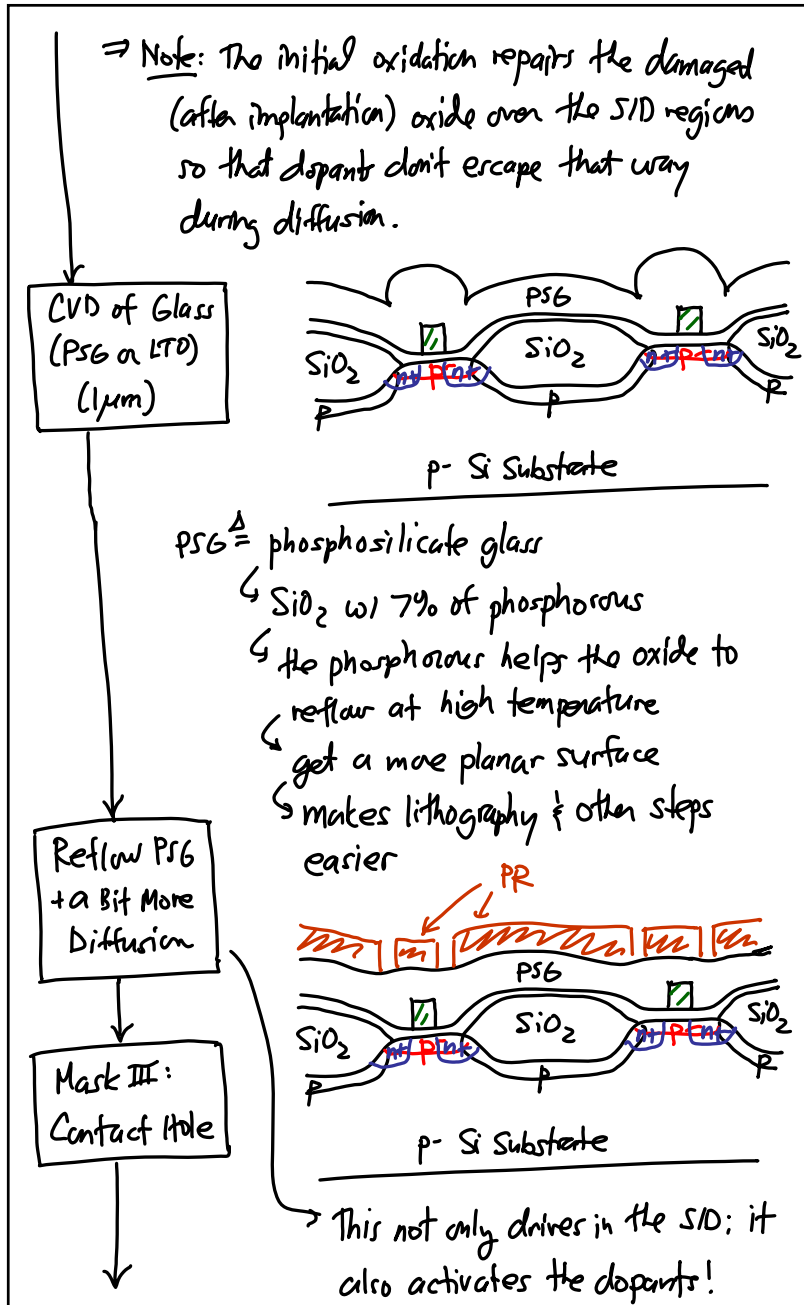
LPCVD Si₃N₄ (100nm)

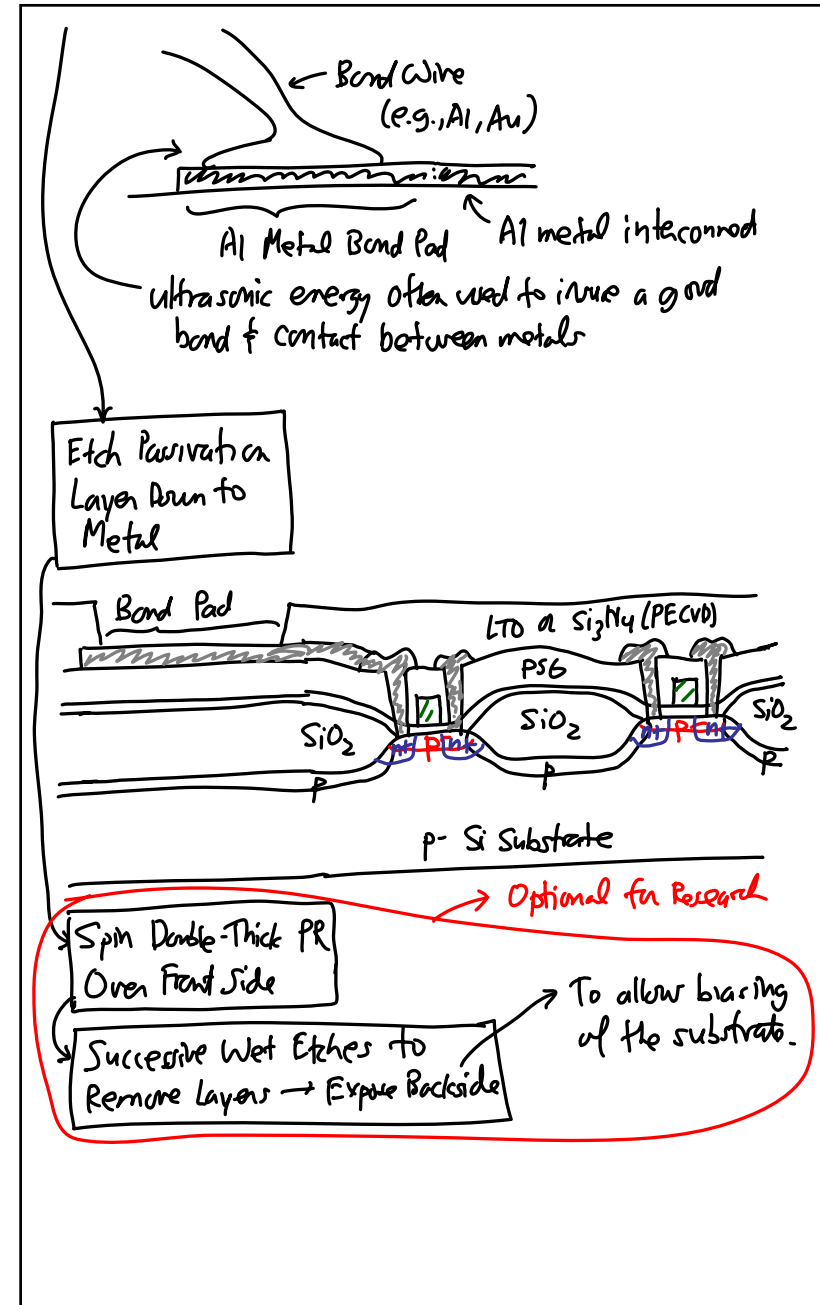
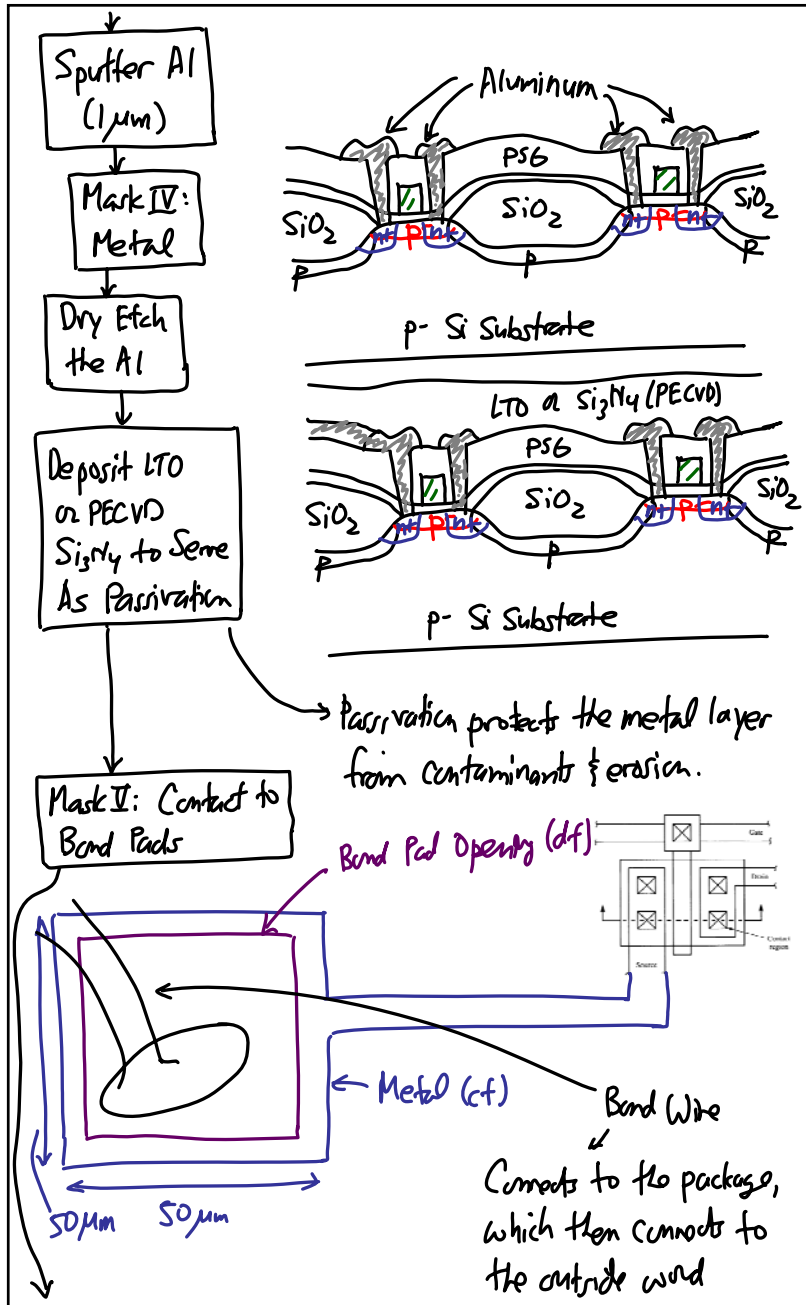
Mask I: Active Region











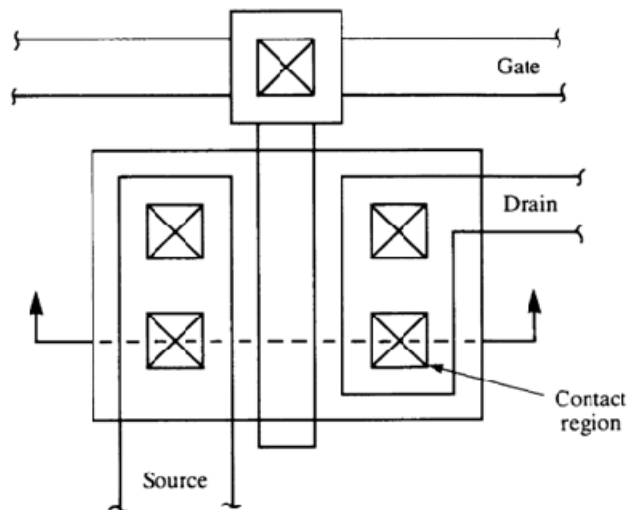
Mark to Cross-Section

⇒ One skill you must learn:

- Given: ① Process Flow
② Mask Layout

Draw the cross-section along various lines and at various steps in the process flow.

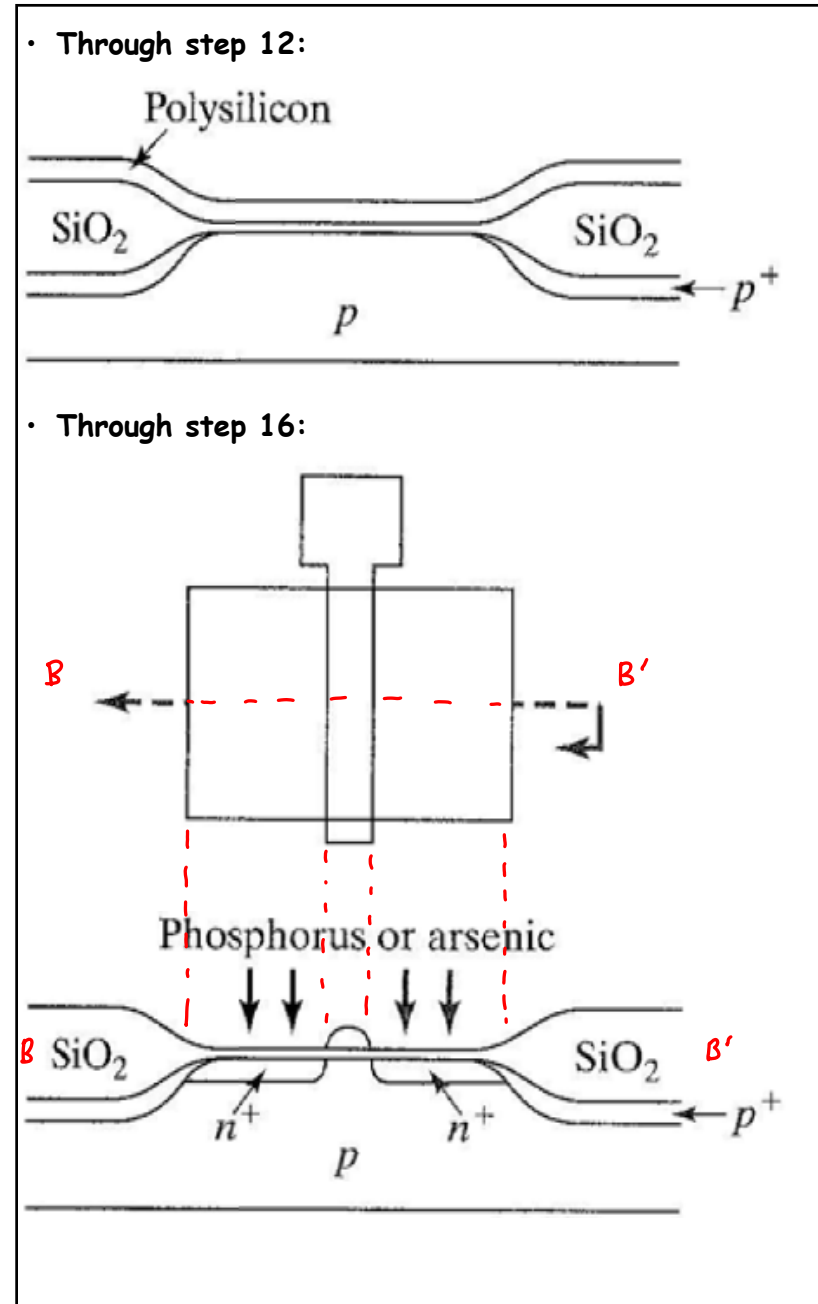
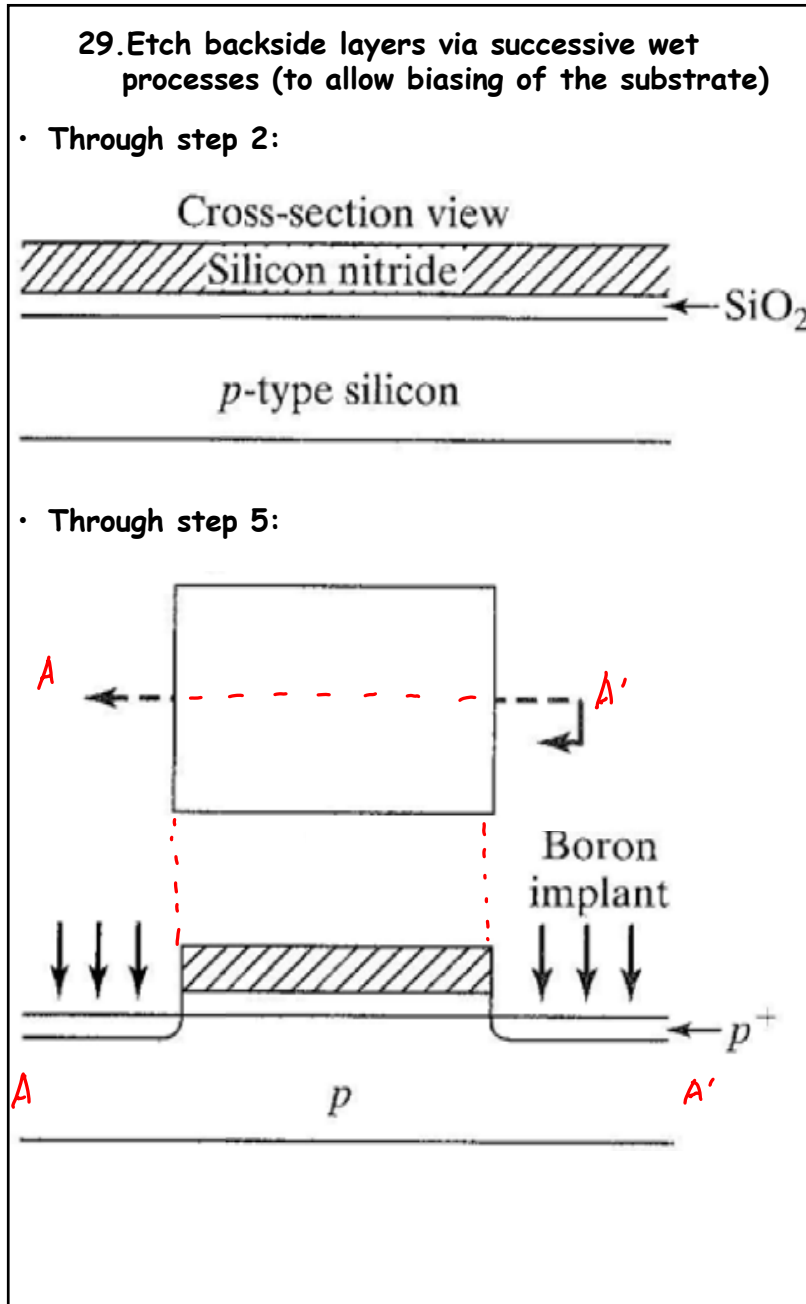
- **Example:** NMOS Process
- **Layout:**



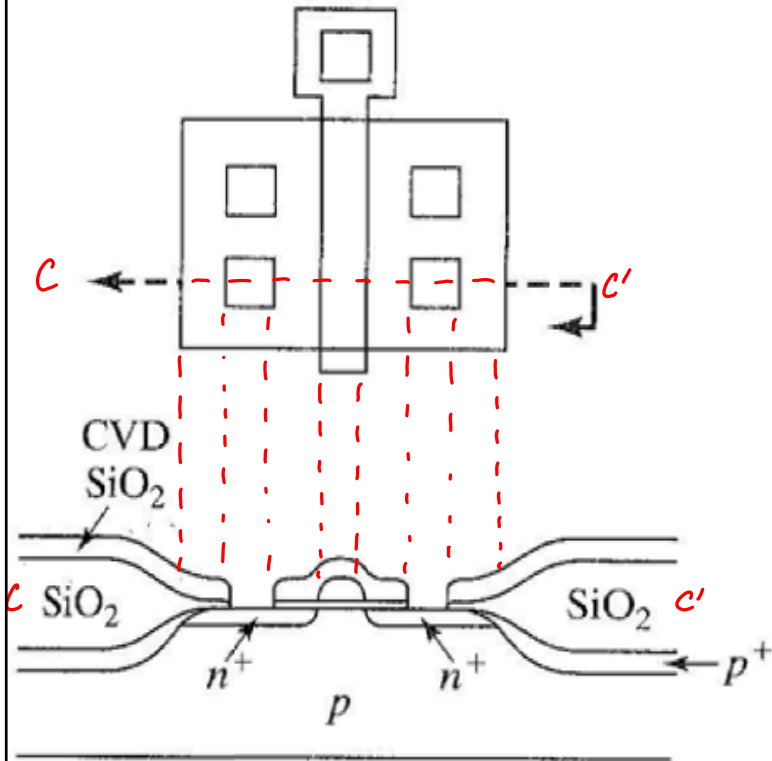
• **Process Flow:**

1. Silicon oxidation: target = 100nm
2. LPCVD Si_3N_4 : target = 100nm
3. Lithography: Mask I (active area)
4. Etch Si_3N_4 to clear it in field areas
5. Field isolation implant: B+ (p-type)

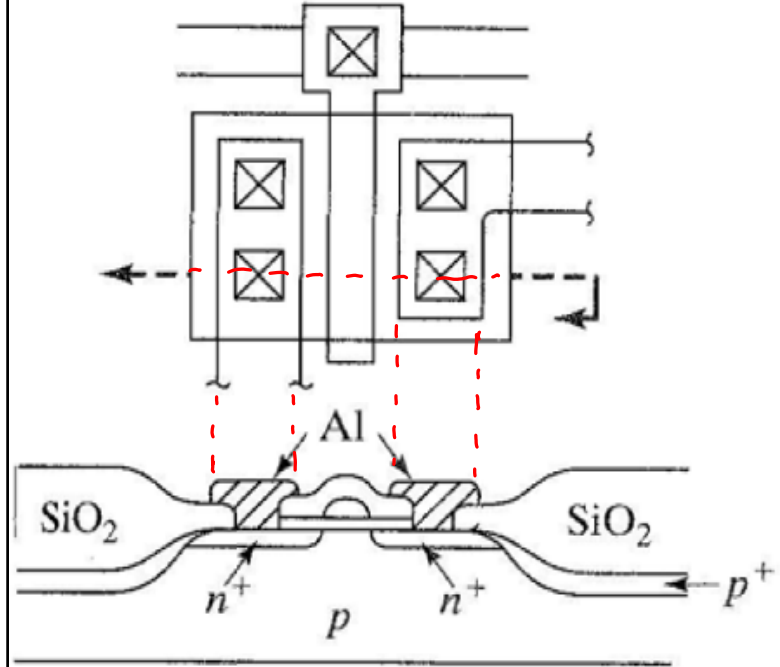
6. Remove PR
7. Grow 1mm of SiO_2 by thermal oxidation (LOCOS oxidation)
8. Blanket etch all Si_3N_4 in hot phosphoric acid wet etchant
9. Threshold voltage implant: B+ (no mask)
10. Remove 100nm of damaged oxide via a timed wet etch in hydrofluoric acid (HF)
11. Grow 100nm of gate thermal oxide in an ultra-clean furnace
12. LPCVD situ phosphorous-doped gate polysilicon
13. Lithography: Mask II (gate polysilicon)
14. Dry etch polysilicon to clear the field areas
15. Remove PR
16. D/S ion implantation: P or As (n-type)
17. Oxidize a bit (10nm) and anneal at 1050°C to activate dopants and drive-in diffusion
18. LPCVD PSG: target = 1μm
19. Reflow PSG (& a little bit of diffusion) at 950°C
20. Lithography: Mask III (contact hole)
21. Dry/wet etch SiO_2 down to n+ S/D regions
22. Sputter Al: target = 1μm
23. Lithography: Mask IV (metal)
24. Dry etch Al
25. Deposit via LTO or PECVD Si_3N_4 to serve as passivation
26. Lithography: Mask V (bond pad contacts)
27. Etch passivation layer down to metal
28. (optional) spin double-thick PR over the front side



• Through step 21:



• Through step 24:



How about a sideways cross-section?

