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# EE 143 Microfabrication Technology Spring 2010

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Lecture Module 7: Interconnects & Contacts

EE 143: Microfabrication Technology LecM 7 C. Nguyen 3/14/10 1

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## Interconnects & Contacts

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## Outline

- Interconnects & Contacts
  - ↳ Planar Process Compatible Metals
  - ↳ Ohmic vs. Diode Contacts
  - ↳ Sintering
  - ↳ Measuring Contact Resistance
  - ↳ Electromigration
  - ↳ Space-Saving Contact Strategies
  - ↳ Silicidation
  - ↳ Lift-Off
  - ↳ Multilevel Metallization
    - ↳ Damascene Process
- Metal MEMS Surface-Micromachining

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## Planar Process Compatible Metals

TABLE 7.1 Bulk Resistivity of Metals ( $\mu\Omega\text{-cm}$ )

Ag: Silver	1.6
Al: Aluminum	2.65
Au: Gold	2.2
Co: Cobalt	6
Cu: Copper	1.7
Mo: Molybdenum	5
Ni: Nickel	7
Pd: Palladium	10
Pt: Platinum	10.6
Ti: Titanium	50
W: Tungsten	5

Source: WebElements (<http://www.webelements.com>)

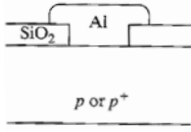
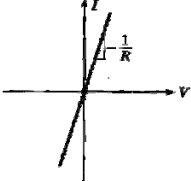
- Aluminum (Al) and gold (Au) used most in IC's before 2002
  - ↳ Al compatible with silicon IC's, so most common on chip
  - ↳ Au not compatible with silicon IC's, since it diffuses too fast and can trap charge; used mainly for bond wires

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### Ohmic Versus Rectifying Contact

**Schottky Ohmic Contact:**

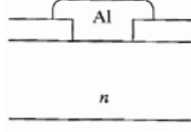
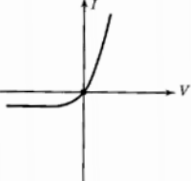
- Metal work function < semiconductor work function
- For Al:  $q\Phi_M = 4.1\text{eV}$
- For p+-Si:  $q\Phi_{Si} \sim 5.17\text{eV}$


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**Schottky Diode Contact:**

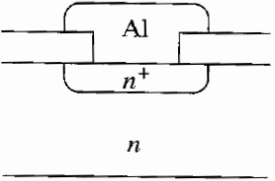
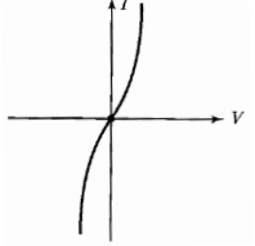
- Metal work function > semiconductor work function
- For Al:  $q\Phi_M = 4.1\text{eV}$
- For n-Si:  $q\Phi_{Si} \sim 4.05\text{eV}$

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### How to Contact n-type?

- Just dope the silicon heavily n-type; i.e., make it n+

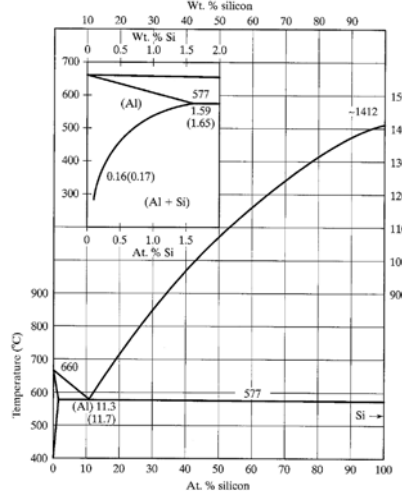



- Depletion region between metal and silicon becomes extremely thin
  - ↳ e-'s can tunnel through it
  - ↳ Basically dope so heavily with n+ that the diode breaks down at a much lower voltage
  - ↳ Gives it an IV-characteristic similar to ohmic

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### Aluminum-Silicon Eutectic Behavior

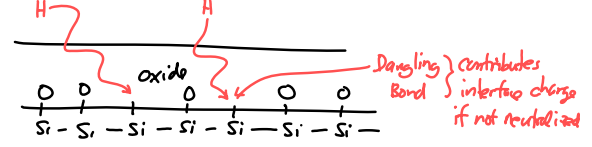
- Silicon melts at 1412°C
- Al melts at 660°C
- But when in contact, Si and Al effectively lower each other's melting temperature
- Minimum temperature is the eutectic temperature that can occur as low as 577°C, where we get 88.7% Al, 11.3% Si



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### Sintering

- Usually need a forming gas anneal @ 400-450°C (called sintering) at the end of an NMOS or CMOS process
  - ↳ Forming gas = mixture of H<sub>2</sub> and N<sub>2</sub>
  - ↳ Improves the metal to silicon contact
  - ↳ Reduces the oxide interface charge, allowing the threshold voltage to be the right value
  - ↳ The H<sub>2</sub> ties up dangling bonds that would otherwise contribute fixed interface charge



- If you finish an MOS process and your thresholds are off, don't despair - just do a sintering step & this will probably fix your problems (almost like magic)

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### Al Spiking & Junction Penetration

- Problem:** taking the temperature up too high causes silicon to diffuse into Al
  - Supply of Si tends to come from a few points, that then leave caves that Al can then go into to form spikes
  - This happens because the silicon wants to diffuse into the Al till it reaches its solid solubility limit of 0.25-1.5%

- To prevent this, can:
  - Incorporate Si into the Al so that it's closer to its solid solubility limit - usually add 1% Si to the Al target in sputtering
  - Use a barrier metal (e.g., TiW)
  - Use a barrier silicide

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### Contact Resistance

- Definition:** Resistance associated with the contact between two materials
- Inversely proportional to the area of the contact

$$R_c = \frac{\rho_c}{A}$$

Specific Contact Resistivity [ $\Omega \cdot \text{cm}^2$ ]  
Contact Resistance  
Contact Area

- Strong function of the sintering temperature

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### Measuring Contact Resistance

- Your lab layout includes contact chains:
  - Metal-Diffusion Contacts
  - Metal-PolySi Contacts

Masks: ACTV POLY CONT METL

- Each chain: 14 series contacts and 7 series resistive pads
- Strategy:** if one uses enough contacts, the contact resistance becomes large enough to measure
- Problem:** segment resistance also rises; how can one delineate the contact resistance?

EE 143: Microfabrication Technology LecM 7 C. Nguyen 3/14/10 11

### Measuring Contact Resistance

- Solution:** use a 4-pt. probe strategy (also on the layout)

Metal-PolySi Contact Resistance Test Structure

Masks: ACTV POLY CONT METL

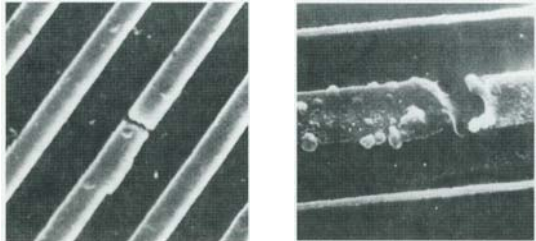
$$R_c = \frac{V}{I}$$

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### Electromigration

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- Definition:** The movement of atoms in a metal film due to momentum transfer from the electrons carrying the current
  - Happens under high current density



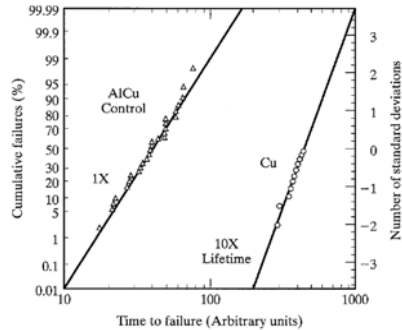
- Mean time to failure (MTF) formula:
 
$$MTF \propto J^{-2} \exp\left[\frac{E_A}{kT}\right]$$
 where
  - $J$  = current density
  - $E_A$  = activation energy (0.4–0.5eV for Al)

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### Electromigration

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- To reduce electromigration can add a small percentage of a heavier metal, like Cu (to Al)
  - Cu has higher mass  $\Rightarrow$  more resistant to electromigration
  - Targets composed of 95% Al, 4% Cu, and 1% Si often used in sputtering systems

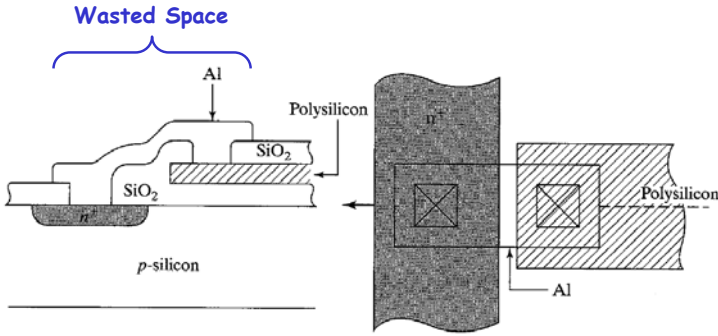


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### Issue: Polysilicon-to-Metal Contact

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- Polysilicon-to-metal contact takes up space
- Need to eliminate waste of space for the smallest circuits, like memory arrays
- Below:** conventional layout

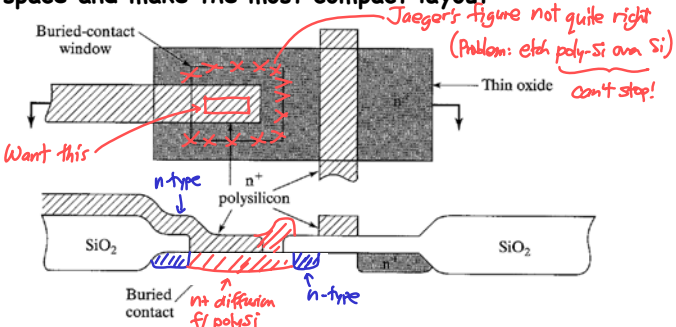


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### Buried Contact

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- Need to add a mask to allow a buried contact, but it can save space and make the most compact layout



- Diffusion from the n+ polySi merges with the S/D diffusion around the gate (the diffusion cannot be initially below the gate, since the gate serves as a mask against the source/drain implant)

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### Butted Contact

- Saves area, since it only needs one contact to connect polysilicon and metal

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### Silicide

- Sheet resistance of polysilicon and shallow diffusions used in CMOS are generally on the order of  $10\text{-}20\Omega/\square$
- Can reduce this resistance to  $15\text{-}50\mu\Omega/\square$  by reacting silicon with a noble or refractory metal to form a silicide

TABLE 7.2 Properties of Some Silicides of Interest. Reprinted with permission of the American Institute of Physics from Ref [4].

Silicide	Starting Form	Sintering Temperature (°C)	Lowest Binary Eutectic Temperature (°C)	Specific Resistivity ( $\mu\text{ohm-cm}$ )
CoSi <sub>2</sub>	Metal on polysilicon	900	1195	18-25
	Cosputtered alloy	900		
HfSi <sub>2</sub>	Metal on polysilicon	900	1300	45-50
MoSi <sub>2</sub>	Cosputtered alloy	1000	1410	100
NiSi <sub>2</sub>	Metal on polysilicon	900	966	50
	Cosputtered alloy	900		50-60
Pd <sub>2</sub> Si	Metal on polysilicon	400	720	30-50
PtSi	Metal on polysilicon	600-800	830	28-35
TaSi <sub>2</sub>	Metal on polysilicon	1000	1385	35-45
	Cosputtered alloy	1000		50-55
TiSi <sub>2</sub>	Metal on polysilicon	900	1330	13-16
	Cosputtered alloy	900		25
WSi <sub>2</sub>	Metal on polysilicon	1000	1440	70
	Cosputtered alloy	1000		35-40
ZrSi <sub>2</sub>	Metal on polysilicon	900	1355	

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### The Silicidation Process

- Expose silicon areas where silicidation is desired
- Blanket deposit metal
- Heat to needed temperature; can be done via rapid thermal anneal (RTA)
- Remove unreacted metal

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### The Silicidation Process

**Remarks:**

- Often can be self aligned to the region to be silicided, in which case it's called a salicide
- Polycide: a silicide over polysilicon
  - Also pretty much self-aligned
  - Just put the metal down everywhere, heat, and reaction will only occur over polysilicon areas
- Achieve resistivities from  $15\text{-}50\mu\Omega\text{-cm}$
- Can oxidize the surface of a silicide, since silicon diffuses through the silicide to combine with the oxidant
- Unlike silicon-metals that are unreacted, many silicides can take temperatures much higher than the eutectic temperature, over  $1000^\circ\text{C}$ 
  - not true for all silicides, e.g., nickel silicide ( $900^\circ\text{C}$ ), platinum silicide ( $800^\circ\text{C}$ ), and palladium silicide ( $700^\circ\text{C}$ )

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### Lift-Off

**Conventional**

(a)

**Lift-Off**

(b)

- Many metals (e.g., nickel, copper) do not have a recipe for dry etching, so cannot be etched anisotropically with good resolution
- Lift-off provides a method for patterning a metal without the need for etching
- **Right:** comparison of conventional and lift-off based metallization processes

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### Multilevel Metallization

- **Big Problem** (for multi-levels of metal): topography
  - ↳ Interferes with lithography, degrading resolution
  - ↳ Creates stringers that then force overetching

- **Solution:** planarization and contact plugs

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### Damascene Process

- Employs plating through molds to achieve contact plugs in a fully-planarized (via CMP) cross-section

(a) Plated copper

(b) Copper Damascene process

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### Dual Damascene Process

- Do multiple steps in one step
- Form interconnect lines and vias between interconnect levels all at the same time

(a)

(b)

(c)

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### Dual Damascene Process

- Do multiple steps in one step
- Form interconnect lines and vias between interconnect levels all at the same time

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### Nickel Surface-Micromachining Process Flow

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### Nickel Metal Surface-Micromachining

- Deposit isolation LTO:
  - Target = 2 $\mu$ m
  - 1 hr. 40 min. LPCVD @450°C
- Densify the LTO
  - Anneal @950°C for 30 min.
- Define metal interconnect via lift-off
  - Spin photoresist and pattern lithographically to open areas where interconnect will stay
  - Evaporate a Ti/Au layer
    - Target = 30nm Ti
    - Target = 270nm Au
  - Remove photoresist in PRS2000  $\rightarrow$  Ti/Au atop the photoresist also removed

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### Nickel Metal Surface-Micromachining

- Evaporate Al to serve as a sacrificial layer
  - Target = 1 $\mu$ m
- Lithography to define anchor openings
- Wet etch the aluminum to form anchor vias
  - Use solution of  $H_3PO_4/HNO_3/H_2O$
- Remove photoresist in PRS2000
- Electroplate nickel to fill the anchor vias
  - Use solution of nickel sulfamate @ 50°C
  - Time the electroplating to planarize the surface

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### Nickel Metal Surface-Micromachining

- Evaporate a thin film of nickel to serve as a seed layer for subsequent Ni electroplating
  - ↳ Target = 20nm
- Form a photoresist mold for subsequent electroplating
  - ↳ Spin 6  $\mu\text{m}$ -thick AZ 9260 photoresist
  - ↳ Lithographically pattern the photoresist to delineate areas where nickel structures are to be formed
- Electroplate nickel structural material through the PR mold
  - ↳ Use a solution of nickel sulfamate @ 50°C
  - ↳ Cathode-to-anode current density  $\sim 2.5 \text{ mA}/\text{cm}^2$

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### Nickel Metal Surface-Micromachining

- Strip the PR in PRS2000
- Remove the Ni seed layer in Ni wet etchant
- Release the structures
  - ↳ Use a  $\text{K}_4\text{Fe}(\text{CN})_6/\text{NaOH}$  etchant that attacks Al while leaving Ni and Au intact
  - ↳ Etch selectivity  $> 100:1$  for Al:Ni and Al:Au

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### Nickel Surface-Micromachining Example

• Below: Surface-micromachined in nickel using the described process flow

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