EECS 16A   Designing Information Devices and Systems I
Fall 2020   Midterm 2 Instructions

Good luck on the midterm! You've studied hard and we are rooting for you to do well! Please read these instructions and the proctoring guidelines before the exam.

Our advice to you: if you can't solve a particular problem, move on to another, or state and solve a simpler one that captures at least some of its essence. You will perhaps find yourself on a path to the solution. **Good luck! We believe in you.**

Format & How to Submit Answers

There are 8 problems (2 introductory questions, and 6 exam questions with subparts) of varying numbers of points on the exam. The problems are of varying difficulty, so pace yourself accordingly and avoid spending too much time on any one question until you have gotten all of the other points you can. If you are having trouble with one problem, there may be easier points available later in the exam!

Complete your exam using either the template provided or appropriately created sheets of paper. Either way, you should submit your answers to the Gradescope assignment that is marked Midterm 2 for your specific exam group. Make sure you submit your assignment to the correct Gradescope assignment. You MUST select pages for each question. We cannot grade your exam if you do not select pages for each question. If you are having technical difficulties submitting your exam, you can email your answers to eecs16a@berkeley.edu.

In general, show all your work legibly to receive full credit; we cannot grade anything that we cannot read. For some problems, we may try to award partial credit for substantial progress on a problem, and showing your work clearly and legibly will help us do that.

Timing & Academic Honesty

You are expected to follow the rules provided in the Exam Proctoring Guidelines (`https://docs. google.com/document/d/1EVb4Ca6FWSAykExY7X5ynFW4KdmHd0BI6KZ0ktM8ows/edit? usp=sharing`). The exam will be available to you at the link sent to you by email. The exam will start at 7pm Pacific Time, Monday, Nov 2nd, 2020, unless you have an exam accommodation. If you experience technical difficulties and cannot access your exam, let us know by making a private post on Piazza and we will try to help.

You have 120 minutes for the exam, with 40 minutes of extra time for scanning and submitting to Gradescope. Most of you will have to submit your exam by 9:40pm unless you have another accommodation. Late submissions will be penalized exponentially. An exam that is submitted N minutes after the end of the submission period will lose 2^N points. This means that if you are 1 minute late you will lose 2 points; if you are 5 minutes late you will lose 32 points and so on.

This is a closed-note, closed-book, closed-internet, and closed-collaboration exam. Calculators are not allowed. You may consult two handwritten 8.5" by 11" cheat sheets (front and back of two pieces of paper). Do not attempt to cheat in any way. We have a zero tolerance policy for violations of the Berkeley Honor Code.

EECS 16A   Designing Information Devices and Systems I
Fall 2020
Midterm 2

1. **HONOR CODE**

   If you have not already done so, please copy the following statements into the box provided for the honor code on your answer sheet, and sign your name.

   I will respect my classmates and the integrity of this exam by following this honor code. I affirm:

   - *I have read the instructions for this exam. I understand them and will follow them.*

   - *All of the work submitted here is my original work.*

   - *I did not reference any sources other than my allocated reference cheat sheet(s).*

   - *I did not collaborate with any other human being on this exam.*

2. (a) **(2 Points) What are you looking forward to after this midterm?** *All answers will be awarded full credit.*

   (b) **(2 Points) Tell us about something that makes you happy.** *All answers will be awarded full credit.*

3. Circuit Analysis (14 points)

(a) (3 points) Which components violate passive sign convention in Fig. 3.1? In your answer sheet, write down all that apply. **For full credit, you must write only components that *violate* passive sign convention. If you list any other components, you will receive no points.**
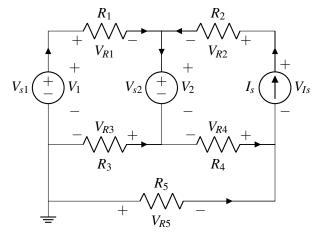

Figure 3.1: Schematic for part (a).

(1) R_1	(3) R_3	(5) R_5	(7) V_{s1}
(2) R_2	(4) R_4	(6) I_s	(8) V_{s2}

(b) (3 points) **Write a KVL expression for the loop drawn in Fig. 3.2. Your answer should be in terms of** $u_1, u_2, u_3, u_4,$ **or** u_5 **and** V_{s1} **and** V_{s2}, please do not add labels to the figure. Show your work.
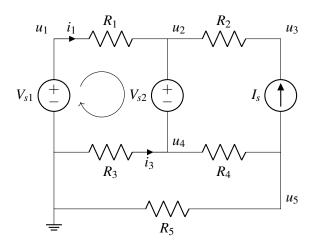

Figure 3.2: Schematic for part (b).

(c) (3 points) **Write the expression** for KCL at node P in terms of currents I_s, i_4, and i_5 as labelled in Fig. 3.3. Then, **re-write the expression** in terms of I_s, node voltages, and resistances only. The rewritten expression should not contain i_4, and i_5. Note that P is a label for a node, and is not a node voltage value. Show your work.
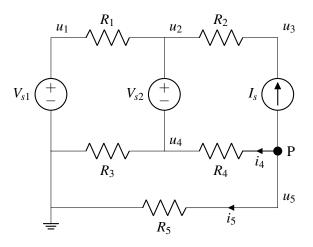

Figure 3.3: Schematic for part (c).

(d) (2 point) Given the node voltage $u_4 = 3V$ in Fig. 3.4, **find the node voltage** u_2. Justify your answer. *Hint: You should not have to do many calculations for this part.*
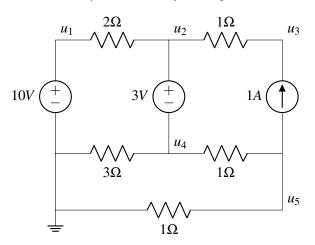

Figure 3.4: Schematic for parts (d) and (e).

(e) (3 point) How would you connect an ammeter to this circuit to measure current flowing through the 3Ω resistor in Fig. 3.4? Recall that an ammeter is a device that measures current, and its symbol is shown in Fig. 3.5. **In your answer sheet, redraw the full schematic from Fig. 3.4 with the ammeter connected correctly.**

Figure 3.5: Ammeter symbol.

4. Take a Load Off (9 points)

Your 16A TA Amanda is an undergraduate researcher in Berkeley's power electronics lab, where she is working on building power converters to drive motors on electric aircraft.

As a part of her project, Amanda is building a piece of test equipment known as a resistive load bank. You are helping her do the calculations!

(a) (2 points) Consider the model in Figure (4.1) for the resistive load bank.

The load resistor $R_L = 100\,\Omega$ and $V_S = 100\,\text{V}$. **When the switch is closed, what is value of the power dissipated by R_L? Show your work.** The switch is ideal for this part, i.e. it acts a wire when it is closed.
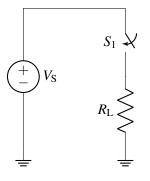

Figure 4.1: Model of resistive load bank in a circuit.

(b) (3 points) Consider again the circuit from Figure (4.1) with the switch closed. Assume that the load resistor $R_L = 100\,\Omega$ can dissipate a max of $P_{max} = 2.5\,\text{kW} = 2.5 \cdot 10^3$ W without exceeding thermal limitations. **What is that maximum value of V_S you can use without exceeding the thermal limits? Show your work.** You may assume the switch is ideal, i.e., it acts a wire when it is closed.

(c) (4 points) For this part, we will no longer assume the switch is ideal; instead, the closed switch has a nonzero on-resistance R_{on}, as shown in Figure (4.2). You found the R_{on} dissipating 2.5 W at load current $I_L = 5\,\text{A}$, as shown in Figure (4.2). **What is the value of R_{on}? Show your work.**
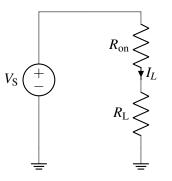

Figure 4.2: Resistive load bank in a circuit with a non-ideal switch.

5. Stay Tuned (15 points)

PG&E just announced another power outage and you desperately need a radio transmitter to battle the impending telecommunication doom! You need to build an antenna tuner, which is a variable resistor to control the power of the transmitter signal.

This tuner consists of two identical resistive bars (M_1 and M_2) of length L, and a cross-sectional area of A, as shown in Figure 5.1. The strips are made of a material with resistivity ρ. The resistive bars are connected with ideal electrical wires in the following configuration:
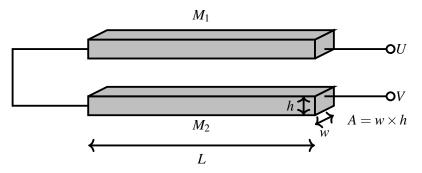

Figure 5.1: Resistive metal bars connected through ideal wires.

(a) (4 points) Let R_{UV} be the equivalent resistance between nodes U and V in Figure 5.1. **Write an expression for R_{UV} in terms of L, A, ρ and other numerical values.** Show your work.

(b) (6 points) The resistive bar M_1 is flexible, so if we press any point on it a contact is made between M_1 and M_2. As shown in Figure 5.2, a sliding contact is used to make a contact at position x_0.
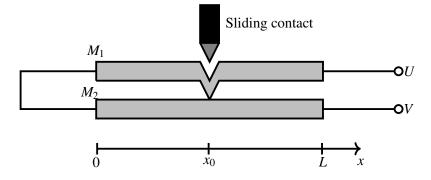

Figure 5.2: Sliding switch making a contact between M_1 and M_2.

(i) **Draw a circuit diagram that represents the scenario in Figure 5.2. The sliding contact has no resistance and acts like a wire when the contact is made.** *Hint: Your diagram should have four resistors.*

(ii) **Express the equivalent resistance between nodes U and V, i.e., R_{UV} in terms of L, x_0, A, ρ and other numerical values, when the sliding contact is present**.

(iii) Assume $x_0 = 8$cm, $L = 10$cm, $A = 10^{-3}$cm^2, and $\rho = 5 \times 10^{-3}\Omega$cm. **Find the value of R_{UV} when the sliding contact is present. Show your work.**

(c) (5 points) Now let us model the transmitter as a voltage source V_S, in series with a resistor R_S, while our antenna tuner is represented by R_{UV}. The circuit model is shown in Figure 5.3:
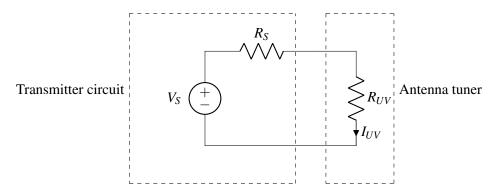

Figure 5.3: Circuit model for the radio transmitter.

In order to prevent damage to the tuner, we need to make sure that the current through R_{UV} never exceeds 0.1A. **Assuming $20\Omega \leq R_{UV} \leq 80\Omega$ and $R_S = 50\Omega$, find the maximum allowable value of V_S, so that $I_{UV} \leq 0.1$A for the full range of R_{UV}. Show your work.**

6. Resistive Touchscreens (15 points)

We have an H-shaped grid of resistors as shown in Fig. 6.1 that we would like to use as a touchscreen. Points P_{00}, P_{10}, P_{01}, P_{11}, P_{02}, and P_{12} are depicted by the black dots. Throughout this question, **measuring a voltage at a certain point means connecting the + terminal of a voltmeter to the black dot corresponding to that point and the − terminal of the voltmeter to the ground node. Note that all resistors are 1kΩ.**

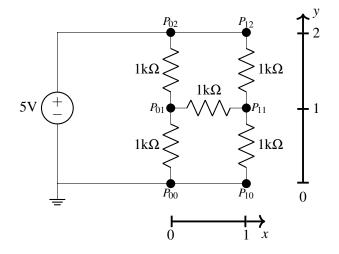Figure 6.1: A schematic of the H-shaped resistive touchscreen.

(a) (3 points) **What are the voltages measured at each of the 6 points P_{00}, P_{10}, P_{01}, P_{11}, P_{02}, and P_{12} in Fig. 6.1? Show your work.**

(b) (3 points) Can we determine the horizontal position (x-coordinate) of touch using this touchscreen in Fig. 6.1? Can we determine the vertical position (y-coordinate) of touch using this touchscreen? **For each direction, if you can, explain why. If you cannot, explain why not.** Note that the x and y axes are drawn on the figure for your convenience.

Question continues on next page.

(c) (6 points) Your friend at Stanford proposes using a different resistive touchscreen shown in Fig. 6.2. **Note that there is a mix of** $1k\Omega$ **and** $2k\Omega$ **resistors, and they accidentally connected a wire between** P_{11} **and** P_{10}.

  (i) Your friend claims to measure a voltage of 0V. Can you identify where the touch happened? If a point exists, write it. If multiple points exist, list them. If no points exist, say so. **Explain your answer.** Note that the measurement circuit is not shown in the figure.

  (ii) Then your friend claims to measure a voltage of 2.5V. Can you identify where the touch happened? If a point exists, write it. If multiple points exist, list them. If no points exist, say so. **Explain your answer.** Note that the measurement circuit is not shown in the figure.
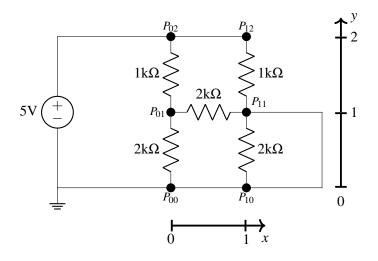

Figure 6.2: A touchscreen proposed by your Stanford friend for part (c).

(d) (3 points) You are now given the resistor grid shown in Fig. 6.3. Your goal is to uniquely determine the horizontal position (x-coordinate) of a touch. How would you connect your voltage source to do this? **In your answer sheet, redraw the full circuit with the voltage source terminals connected to the correct nodes.**
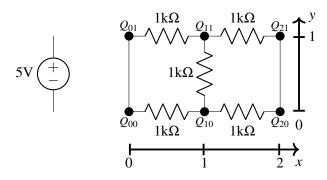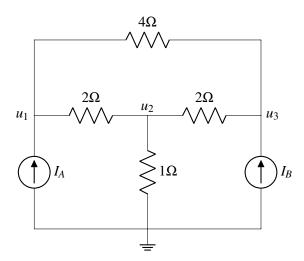

Figure 6.3: Resistor grid for part (d).

7. Superposition (23 points)

For this question, we will analyze the circuit shown below with the two current sources of strength I_A and I_B as inputs. It may be observed that the network of resistors shown in the circuit is symmetric. We will first solve this circuit for symmetric inputs $I_A = I_B$, and then for anti-symmetric inputs $I_A = -I_B$. Using these two results, we we will solve the circuit for arbitrary inputs I_A, I_B.

(a) (6 points) Consider the following circuit in Fig. 7.1 with symmetric inputs, $I_A = I_B = 1A$. **Using superposition, solve for the node voltages at the nodes marked u_1, u_2 and u_3.** Show your work and justify your answer.

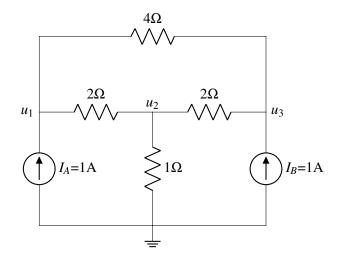(*Hint: You should find that the node voltages u_1 and u_3 will be the same, that is, $u_1 = u_3$.*)

Figure 7.1: Schematic for part (a).

(b) (6 points) Consider the following circuit in Fig. 7.2 with anti-symmetric inputs, $I_A = 1\,\text{A}$ and $I_B = -1\,\text{A}$. **Using superposition solve for the node voltages at the nodes marked u_1, u_2 and u_3.** Show your work and justify your answer.
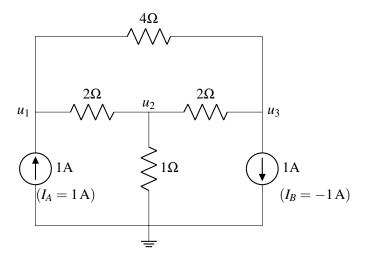
(*Hint: You should find that $u_1 = -u_3$.*)

Figure 7.2: Schematic for part (b).

(c) (3 points)

Now consider Fig. 7.3, where $I_A = 2\,\text{A}$ and $I_B = 2\,\text{A}$; in other words, we double the current sources from part (a). Here, as well as in the earlier circuits, the node voltages u_1, u_2 and u_3 can be represented by the vector $\vec{u} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix}$.

Assume that when $I_A = 1\,\text{A}$ and $I_B = 1\,\text{A}$ as part (a), the solution was given by $\vec{u} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} = \begin{bmatrix} \alpha \\ \beta \\ \alpha \end{bmatrix}$.

What are the new node voltages, $\vec{u} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix}$, in Fig. 7.3, when $I_A = 2\,\text{A}$ and $I_B = 2\,\text{A}$? Write your answer in terms of α and β. You do not need to use any of the work from parts (a) and (b) to solve this part. Justify your answer.

Hint: It might be helpful to think of the circuit as being represented by a system of equations given as:

$$A\vec{u} = \vec{b},$$

where $A \in \mathbb{R}^{3\times 3}$, $\vec{u} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix}$ and $\vec{b} = \begin{bmatrix} I_A \\ 0 \\ I_B \end{bmatrix}$. However, you do not need to find A to solve this problem.
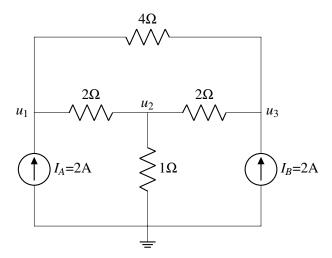

Figure 7.3: Schematic for part (c).

(d) (8 points) Assume that when $I_A = 1\,\mathrm{A}$ and $I_B = 1\,\mathrm{A}$ (also known as "common mode"), the node voltages were given by $\vec{u}_{cm} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} = \begin{bmatrix} \alpha \\ \beta \\ \alpha \end{bmatrix}$. Also, assume that when $I_A = 1\,\mathrm{A}$ and $I_B = -1\,\mathrm{A}$ (also known as

"differential mode"), the node voltages were given by $\vec{u}_{dm} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} = \begin{bmatrix} \gamma \\ 0 \\ -\gamma \end{bmatrix}$.

Consider the circuit shown below in Fig. 7.4, **with current sources of strengths $I_A = 6\mathrm{A}$ and $I_B = 2\mathrm{A}$.**

Find the node voltages, $\vec{u} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix}$, in terms of α, β and γ. You do not need to use any of the work from parts (a) and (b) to solve this part. Show your work and justify your answer. You do not have to use to NVA to solve this part, there is an easier solution.
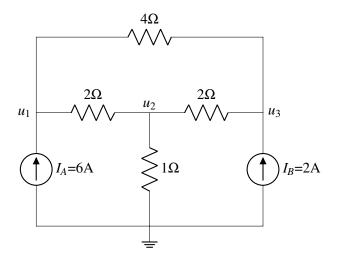

Figure 7.4: Schematic for part (d).

Hint: Again, as before, it might be helpful to think of the circuit as being represented by a system of equations given as:

$$A\vec{u} = \vec{b},$$

where $A \in \mathbb{R}^{3\times3}$, $\vec{u} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix}$ and $\vec{b} = \begin{bmatrix} I_A \\ 0 \\ I_B \end{bmatrix}$. However, you do not need to find A to solve this problem.

Can you write $\vec{b}$ as a linear combination of two vectors that correspond to the circuits you have already solved?

8. DRAM (Dynamic Random Access Memory) Cell (28 points)

You are on a research team investigating the design of Dynamic Random Access Memory (DRAM) cells to improve their performance!
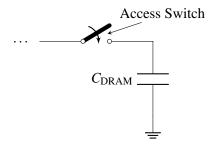

Figure 8.1: A DRAM cell consisting of an access switch and a capacitive storage element, C_{DRAM}.

(a) (3 points) You are making a capacitor with a new insulating material between the DRAM capacitor plates. The DRAM capacitor has the following properties:

- C_{DRAM} plate area, $A = 1\,\mu\text{m} \times 10\,\mu\text{m} = 10^{-11}\text{m}^2$,
- Distance between C_{DRAM} plates, $d = 40\,\text{nm} = 4 \times 10^{-8}\text{m}$,
- Permittivity of the material between the C_{DRAM} plates, $\varepsilon = 40\varepsilon_0$ F/m, where ε_0 is the permittivity of free space.

What is the capacitance of a DRAM capacitor, $C_{\mathbf{DRAM}}$, in terms of ε_0 and other numerical values. Show your work. You do not need to substitute the value of ε_0.

(b) (3 points) Now let's consider the case in Figure 8.2, which is the setup after the switch in Figure 8.1 is closed at time $t = 0$. When the switch is closed it starts conducting a current I_{switch}, as shown in Figure 8.2.

Assume that C_{DRAM} has no charge stored on it at $t = 0$ seconds, i.e. it has no initial charge. Let $I_{\text{switch}} = 90\,\text{pA} = 9 \times 10^{-11}\text{A}$, and $C_{\mathrm{DRAM}} = 90\,\text{fF} = 9 \times 10^{-14}\text{F}$.

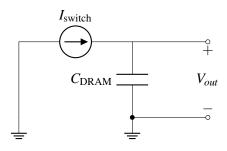**Find the value of V_{out} at $t = 1\,\text{ms} = 10^{-3}\text{s}$. Show your work.**

Figure 8.2: Ideal DRAM cell.

(c) (5 points) Unfortunately, in reality, our access switch is not ideal and has a *parasitic capacitance* C_{switch}, which gets added to the circuit when the switch is closed. C_{switch} affects the DRAM write speed, i.e. how fast C_{DRAM} can be charged.

Find rate of change of V_{out}, i.e. $\frac{dV_{out}}{dt}$, as a function of C_{DRAM}, C_{switch} and I_{switch} for both (i) the ideal circuit circuit without C_{switch}, as shown in the left side of Figure 8.3 and (ii) the non-ideal circuit circuit with C_{switch}, as shown in the right side of Figure 8.3. Show your work.

Then compare $\frac{dV_{out}}{dt}$ values for both circuits. A larger $\frac{dV_{out}}{dt}$ means faster write speed.

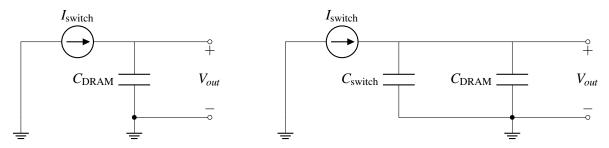**Which circuit has faster write speed? Justify your answer.**

Figure 8.3: Left: Circuit without parasitic capacitance.   Right: Circuit with parasitic capacitance.

(d) (3 points) Assume you want to build an array of DRAM capacitors. You start by connecting two DRAM capacitors in parallel and charging them with a voltage source with value V_{DD}, as shown in Figure 8.4. Each DRAM capacitor has a capacitance value of C_{DRAM}.
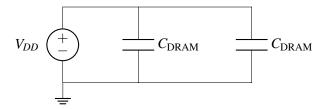

Figure 8.4: DRAM capacitors in parallel are charged.

When the capacitors are charged, how much total energy is going to be stored in both DRAM capacitors together? Show your work. Your answer should be a function of C_{DRAM} and V_{DD}.

(e) (6 points) Finally! You make it to the lab! Unfortunately, you accidentally wind up introducing an additional capacitive component, C_{mistake}.

Before your grad student mentor finds out your mistake, you'd like to quickly add an additional capacitor C_{fix}, as shown in in Figure 8.5, so that the equivalent capacitance between nodes a and b becomes the same as C_{DRAM}.

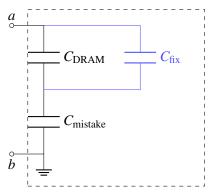

Figure 8.5: Your fabricated DRAM cell with an additional mistake capacitance, C_{mistake}, and a capacitance intentionally added to fix the mistake, C_{fix}.

Find the expression for C_{fix} so that the equivalent capacitance between nodes a and b is C_{DRAM}. Assume $C_{\text{mistake}} > C_{\text{DRAM}}$. Show your work. Your answer should be in terms of C_{DRAM} and C_{mistake}.

Hint: You can start by expressing equivalent capacitance of the network in the dashed box as a function of C_{DRAM}, C_{fix} and $C_{mistake}$.

(f) (8 points) You made two DRAM cells, but due to some unfortunate error you end up with: $C_1 = \frac{C_{\text{DRAM}}}{4}$ and $C_2 = C_{\text{DRAM}}$. You charge up C_1 to test it and have placed initial voltage $V_1(0) = V_{DD}$ on it. The second capacitor C_2 has not been charged yet and the initial voltage on C_2 is $V_2(0) = 0\,\text{V}$.

Now you close S_2 at $t = 0$ so that C_2 can share charge from C_1, while S_1 remains closed, as in Fig. 8.6.

Find V_1 and V_2 at steady-state after switch S_2 is closed and switch S_1 remains closed. Your final answer should be in terms of C_{DRAM} and V_{DD}. Show your work and justify your answer.
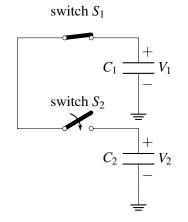

Figure 8.6: Two DRAM cells in parallel. Switch S_1 is closed (can be thought of as a wire), and switch S_2 is closing.