EECS 16A Designing Information Devices and Systems I
Spring 2023 Midterm 2

PRINT your student ID: ____

PRINT AND SIGN your name: ____________________, ____________________ ________________________
(last name) (first name) (signature)

PRINT the time of your discussion section and your GSI(s) name: ____

PRINT the student IDs of the person sitting on your right: ___________________ and left: ___________________

General Notes

- This exam has a combination of multiple choice, fill in the blank, and free response questions.
- This exam will be partially auto-graded. **You must adhere to the following format to receive full credit:**
  - For fill in the blank and free response questions, **legibly write your final answer entirely in the provided boxes**. Any work done outside of the provided boxes will not be graded.
  - For multiple choice questions, select exactly *one* choice by filling the bubble ●.
    ◯ You must choose either this option. ◯ Or this one, but not both!

1. HONOR CODE

Please read the following statements of the honor code, and sign your name (you don't need to copy it).

I will respect my classmates and the integrity of this exam by following this honor code. I affirm:

- *I have read the instructions for this exam. I understand them and will follow them.*
- *All of the work submitted here is my original work.*
- *I did not reference any sources other than my unlimited printed resources.*
- *I did not collaborate with any other human being on this exam.*

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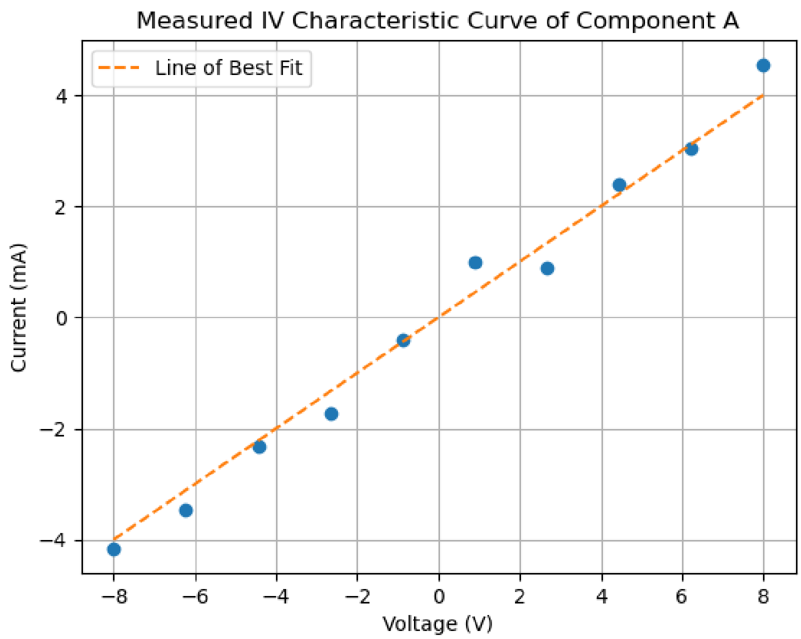
2. Characterizing Components (13 Points)

Your lab TA has been exploring the 16A lab and discovered a bin of unlabeled components. She has collected some data about these mysterious components, and needs your help to interpret them.

(a) (3 points) She begins with a mysterious two-terminal component and labels it ‘Component A’. After connecting it to one of the signal generators in the lab, she measures many voltage and current points forming an approximate I-V curve.



i. Which circuit element best describes Component A?

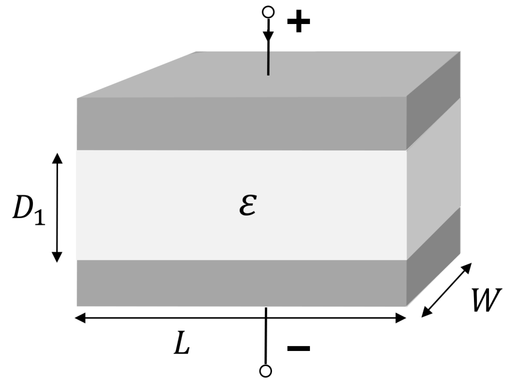
◯ Resistor
◯ Capacitor
◯ Voltage Source
◯ Current Source
◯ Open Circuit
◯ Short Circuit

ii. Paying careful attention to the measured units of current and voltage, express both the numeric value of the circuit element and its corresponding units (from the options provided).

[ ]

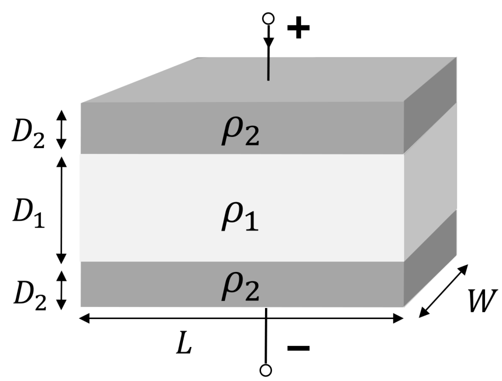
◯ Volts (V)
◯ Amps (A)
◯ Ohms (Ω)
◯ Farads (F)

(b) (2 points) Your TA picks a different component out of the bin and labels it 'Component B'. She finds a corresponding datasheet which provides information on its structure and properties. It states that Component B *is a parallel plate capacitor*, which is physically modeled with three layers as follows:



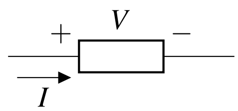
Write an expression for the capacitance of Component B as a function of dielectric permittivity ε and dimensions D_1, L, and W.

(c) (3 points) In the course of testing, your TA connected a large voltage source and put too much power through the capacitor. This resulted in the dielectric (the middle layer) breaking down, so that the entire three-layer device *behaves like a resistor*. After degradation, the device can be modeled as:



Write an expression for the *resistance* of Component B as a function of D_1, D_2, L, W, and resistivities ρ_1 and ρ_2.

(d) (5 points) Your lab TA decides to try characterizing one final component and labels it 'Component C'. She connects Component C to a circuit and measures the voltage across it and current through it as shown



From her measurement she finds that $I = -5\,\mu\text{A}$ and $V = 0.2\,\text{V}$.

i. Is Component C labeled according to passive sign convention?

◯ Yes ◯ No

ii. What is the power *dissipated* by Component C?

μW

iii. Is Component C consuming or generating power?

◯ Consuming ◯ Generating

iv. Regardless of your answers to the previous parts, assume Component C generates a constant $10\,\mu\text{W}$ of power and is connected to a 1 mWh battery (a 'Wh' or 'watt-hour' is a unit of energy). How long will it take to charge the battery from 0 to 100% capacity?

hours

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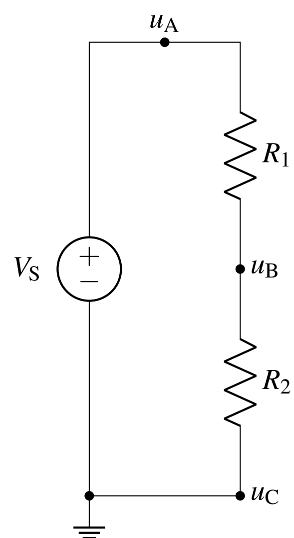
3. Can You Divide a Divider? (16 Points)

For all parts please give your **answer in terms of the labeled circuit quantities**. When expressing your answers, you are free to use the parallel (‖) operator.

(a) (4 points) Consider the circuit below.

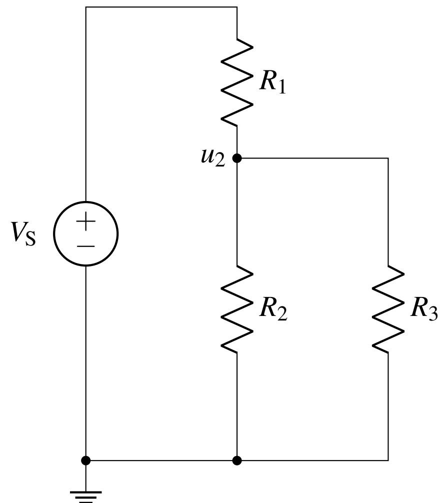


i. Find the voltage at node u_B as a function of V_S, R_1, and R_2.

ii. How would you attach a voltmeter to check your answer for node voltage u_B? Indicate the **nodes** (i.e., u_A, u_B, or u_C) you would connect to each voltmeter terminal.

positive voltmeter terminal: ☐ negative voltmeter terminal: ☐

(b) (4 points) Now consider a new circuit.

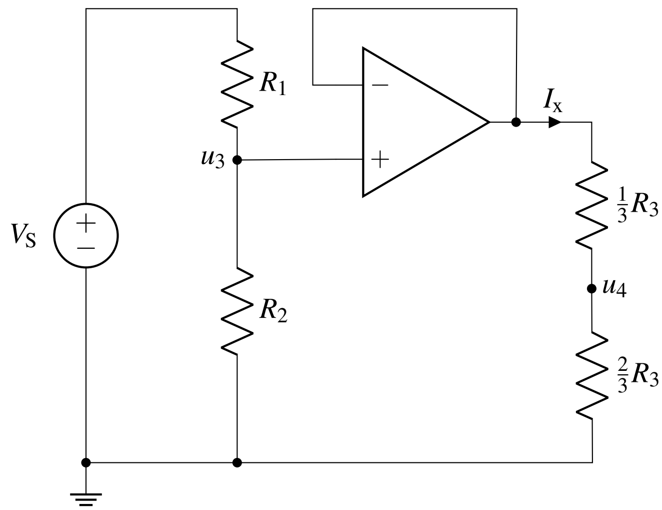


i. Find the voltage at node u_2 as a function of V_S, R_1, R_2, and R_3.

ii. How does the node voltage u_2 compare to the node voltage u_B in part (a)? Using 1-2 sentences, provide a conceptual reason for your answer.

○ $u_2 > u_B$ ○ $u_2 = u_B$ ○ $u_2 < u_B$

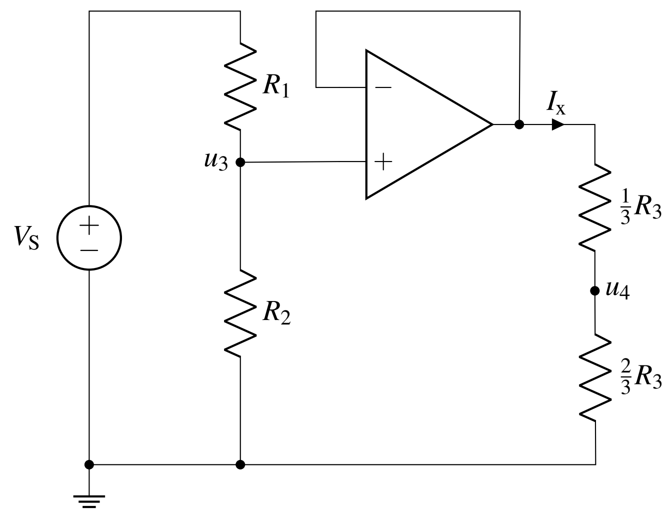
(c) (8 points) Now consider a new circuit shown below. Assume the op-amp is ideal and in negative feedback.



i. Find an expression for the voltage at u_3 as a function of V_S, R_1, R_2, and R_3.

ii. How does the node voltage u_3 compare to the node voltage u_2 in part (b)? Using 1-2 sentences, provide a conceptual reason for your answer.

○ $u_3 > u_2$ ○ $u_3 = u_2$ ○ $u_3 < u_2$



iii. Find an expression for the voltage at u_4 as a function of V_S, R_1, R_2, and R_3. Your answer should NOT include any node voltages (i.e., u_3)

iv. Find an expression for the current I_x as a function of V_S, R_1, R_2, and R_3. Your answer should NOT include any node voltages (i.e., u_3).

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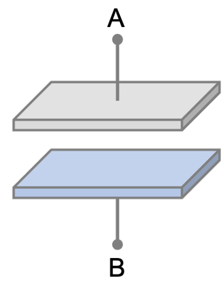
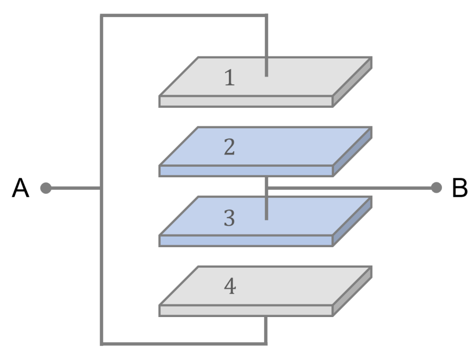
4. Stacked Capacitors (11 points)

The parallel plate capacitor shown below is made up of two identical perfectly overlapping plates. The plates have length l, width w, are separated by distance d, and the dielectric material between the plates has permittivity ε. The capacitance formed by the two plates between nodes **A** and **B** is C_0.



(a) (3 points) Now assuming these same specifications, we stack 4 plates on top of each other. The plates are perfectly aligned vertically and the spacing between each plate is d. We connect node **A** to the top and bottom plates and node **B** to the middle two plates.



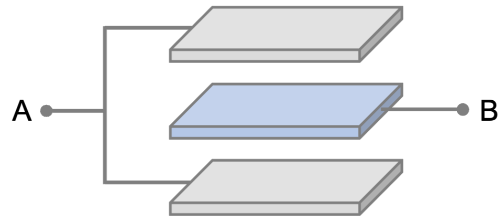
i. Is there capacitance formed between the 2nd and 3rd plates?

◯ Yes ◯ No

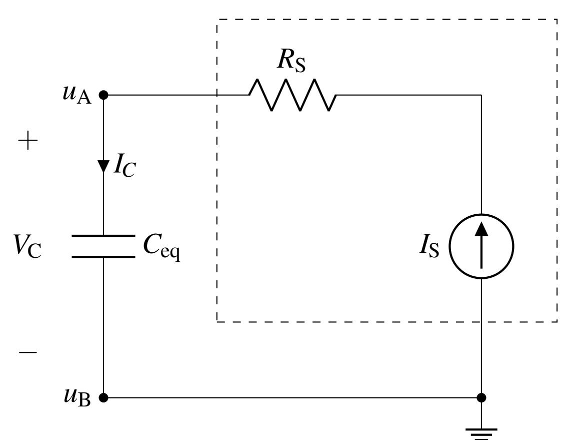
ii. Draw an equivalent capacitor circuit representing this physical arrangement of plates. Label nodes **A** and **B**.

(b) (2 points) From the capacitor configuration in part (a), we combine the two middle plates into a single plate. Assume all other specifications are the same as in part (a).

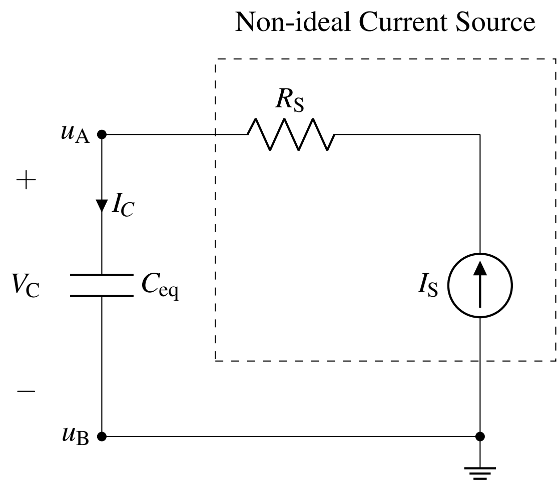
Find C_{eq}, the equivalent capacitance between nodes **A** and **B**. Express your answer in terms of C_0 (the equivalent capacitance of just two plates).



(c) (6 points) We want to charge up our stacked capacitor, C_{eq}, with a current source. Unfortunately our current source is non-ideal, and instead can be modeled by an ideal current source, I_{S}, and a resistor, R_{S}, in series. The capacitor C_{eq} is uncharged at time $t = 0$.



i. Find an expression for the power dissipated by resistor R_{S} in terms of C_{eq}, I_{S}, R_{S}, and t.



ii. Find the node voltage $u_A(t)$ in terms of C_{eq}, I_S, R_S, and t.

iii. Find an expression for the power delivered to the capacitor C_{eq} in terms of C_{eq}, I_S, R_S, and t. The capacitor voltage V_C and current I_C are labeled for you.

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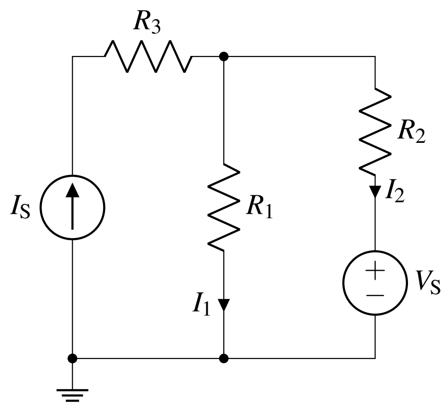
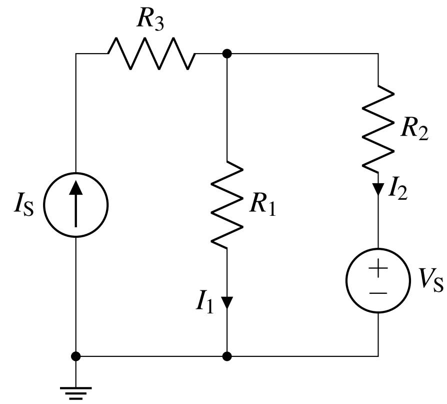
5. A Plain Circuit (16 points)

Consider the following circuit



(a) (3 points) Find the current I_1 passing through the resistor R_1 with the **current source turned on** and the **voltage source turned off**. Your answer must be *only* in terms of I_S, V_S, R_1, R_2, and R_3.

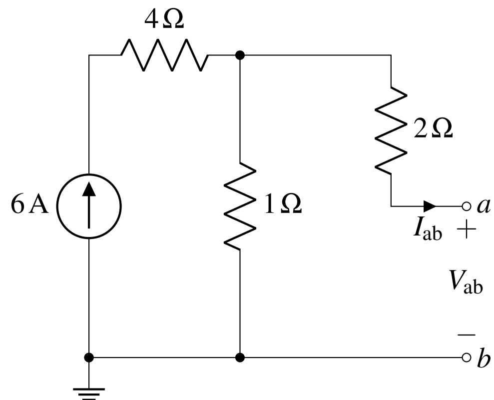
(b) (3 points) Find the current I_1 passing through the resistor R_1 with the **current source turned off** and the **voltage source turned on**. Your answer must be *only* in terms of I_S, V_S, R_1, R_2, and R_3.



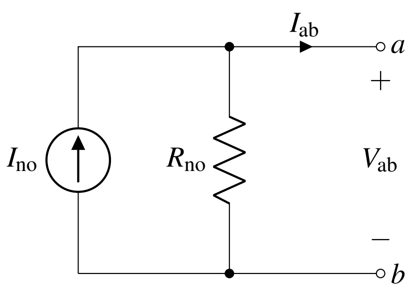
(c) (2 points) Using the principle of *superposition*, find the total current I_1 passing through the resistor R_1 when **both** the current source and voltage source are turned on. Your answer must be *only* in terms of I_S, V_S, R_1, R_2, and R_3.

(d) (2 points) Redraw the circuit but with an ammeter added to measure the current I_2. Be sure to notate the direction of positive current for the ammeter.

(e) (4 points) Now you want to determine the equivalent circuit seen from the voltage source V_S. You remove the voltage source from the circuit. You also now know the numerical values of the current source I_S and resistances R_1, R_2, and R_3.

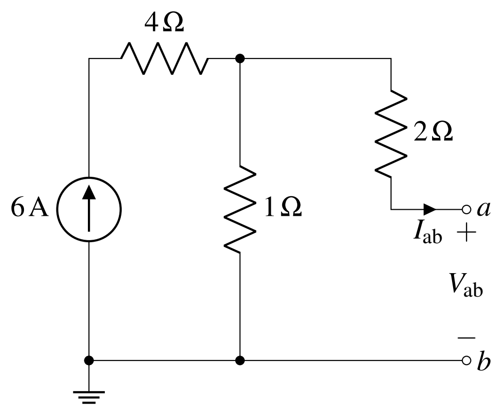


For this circuit, derive the Norton equivalent between nodes a and b. Find the Norton current, I_{no}, and the Norton resistance, R_{no}.



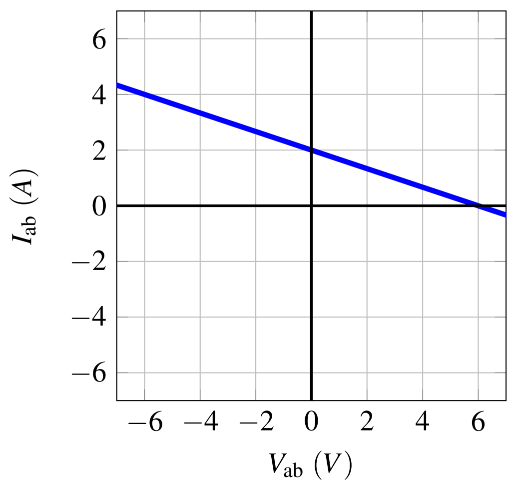
I_{no} = [ ] A

R_{no} = [ ] Ω



(f) (2 points) For the circuit in part (e), select the line which represents the I-V characteristic at terminals a and b (i.e., I_{ab} vs V_{ab})?

○



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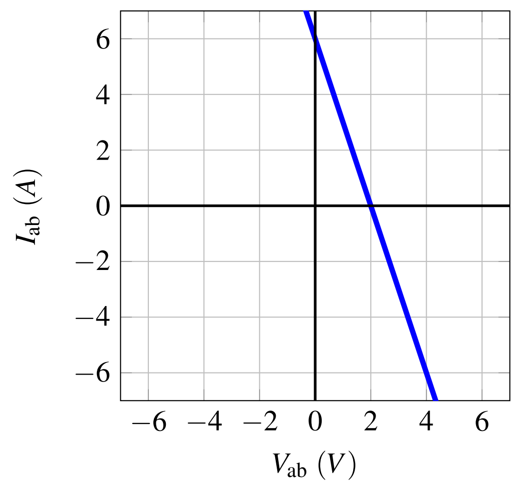

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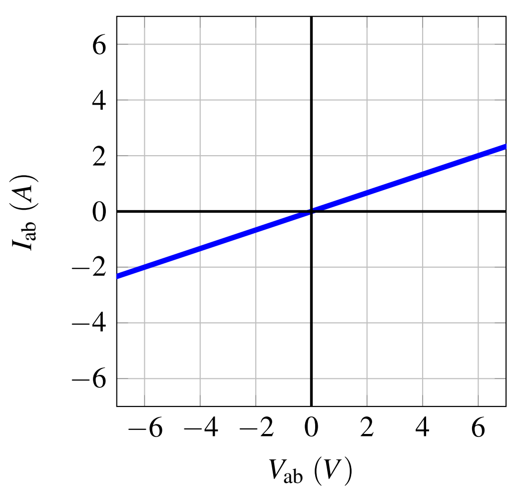

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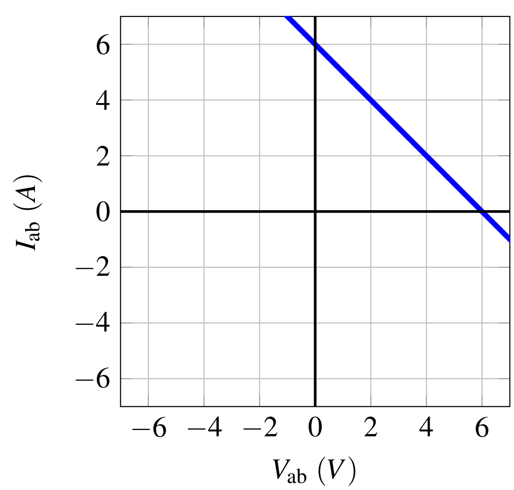

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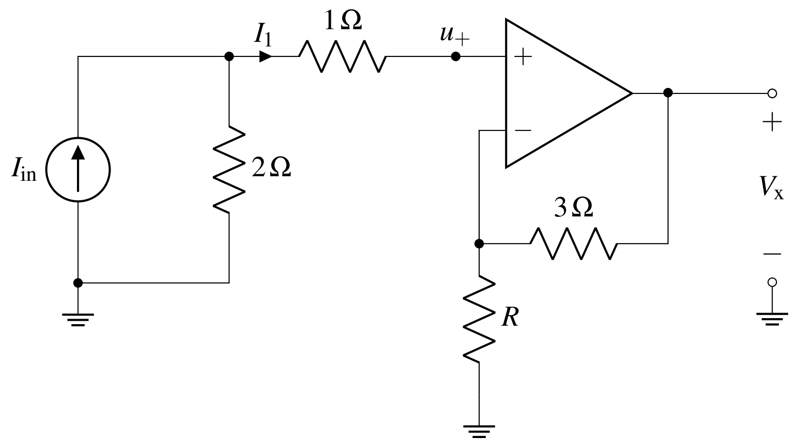
6. Does The Circuit Blink? (17 points)

Consider the following circuit with an ideal op-amp



(a) (2 point) Is the op-amp configured in positive or negative feedback?

◯ Positive feedback ◯ Negative feedback

(b) (2 points) If $I_{\text{in}} = 1\,\text{A}$, then what is value of the current I_1?

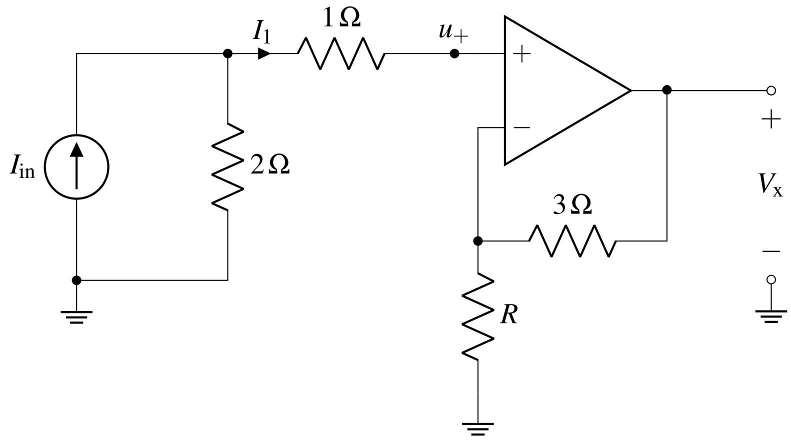
$I_1 =$ [ ] A

[ ]

(c) (2 points) If $I_{\text{in}} = 1\,\text{A}$, derive the voltage at node u_+.

$u_+ =$ [ ] V

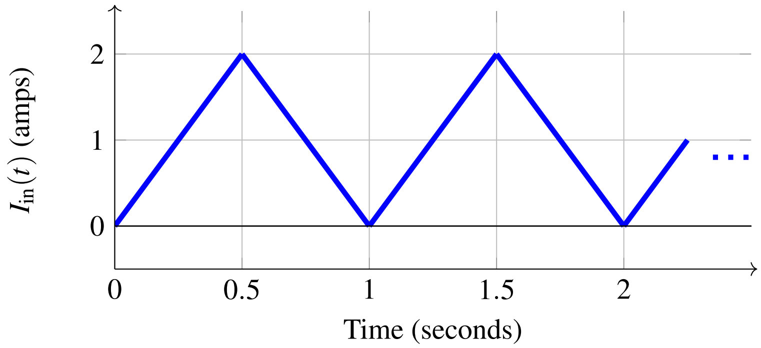
[ ]

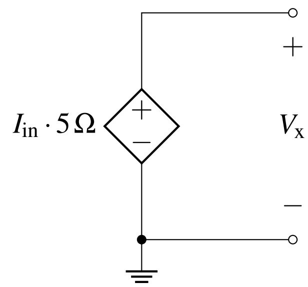


(d) (3 points) Determine the value of resistor R so that $V_{\mathrm{x}} = I_{\mathrm{in}} \cdot 5\,\Omega$.

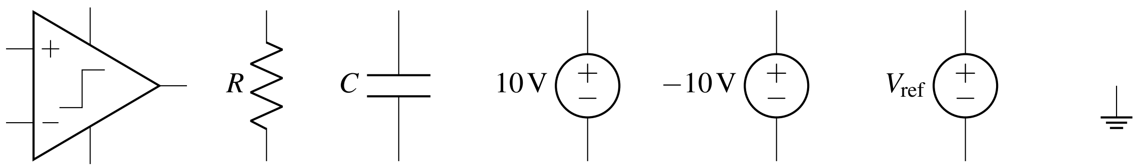
$R =$ $\square$ Ω

(e) (8 points) Now the input current $I_{in}(t)$ has the following triangular waveform with time. Regardless of your answer to the previous parts, assume you have successfully implemented the function of the circuit: $V_x = I_{in} \cdot 5\,\Omega$. Then the op-amp circuit can be represented with an equivalent circuit as shown.





Using the voltage V_x as an input, design a comparator circuit that creates an output voltage $V_{out}(t)$ alternating periodically between a low voltage $-10\,\text{V}$ and high voltage $+10\,\text{V}$ with *equal durations*. You do not have to use every element and you can use multiple of each element. **If used, also specify your chosen values of R, C, and V_{ref} for each element.** Be sure to not leave any circuit element terminals unconnected.



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Extra page for scratchwork.
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