EECS 16A Designing Information Devices and Systems I
Spring 2023 Midterm 2

Midterm 2 Solution

General Notes

- This exam has a combination of multiple choice, fill in the blank, and free response questions.
- This exam will be partially auto-graded. **You must adhere to the following format to receive full credit:**
  - For fill in the blank and free response questions, **legibly write your final answer entirely in the provided boxes**. Any work done outside of the provided boxes will not be graded.
  - For multiple choice questions, select exactly *one* choice by filling the bubble ●.
    ◯ You must choose either this option. ◯ Or this one, but not both!

1. HONOR CODE

Please read the following statements of the honor code, and sign your name (you don't need to copy it).

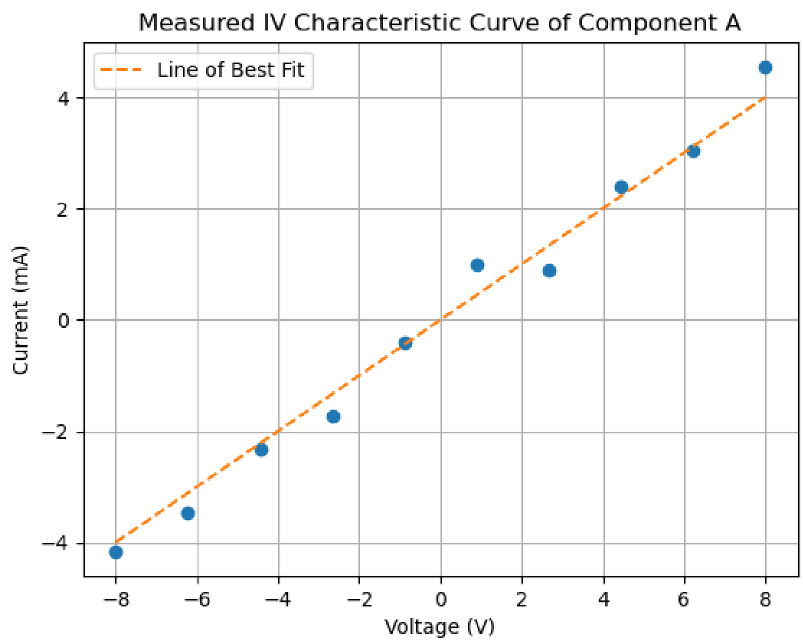
I will respect my classmates and the integrity of this exam by following this honor code. I affirm:

- *I have read the instructions for this exam. I understand them and will follow them.*
- *All of the work submitted here is my original work.*
- *I did not reference any sources other than my unlimited printed resources.*
- *I did not collaborate with any other human being on this exam.*

2. Characterizing Components (13 Points)

Your lab TA has been exploring the 16A lab and discovered a bin of unlabeled components. She has collected some data about these mysterious components, and needs your help to interpret them.

(a) (3 points) She begins with a mysterious two-terminal component and labels it 'Component A'. After connecting it to one of the signal generators in the lab, she measures many voltage and current points forming an approximate I-V curve.



i. Which circuit element best describes Component A?

- ● Resistor
- ○ Capacitor
- ○ Voltage Source
- ○ Current Source
- ○ Open Circuit
- ○ Short Circuit

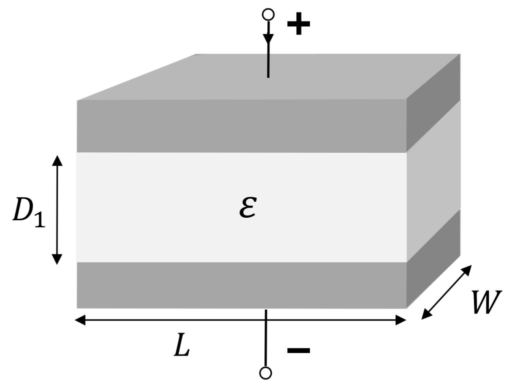
ii. Paying careful attention to the measured units of current and voltage, express both the numeric value of the circuit element and its corresponding units (from the options provided).

Solution:

2000

- ○ Volts (V)
- ○ Amps (A)
- ● Ohms (Ω)
- ○ Farads (F)

(b) (2 points) Your TA picks a different component out of the bin and labels it 'Component B'. She finds a corresponding datasheet which provides information on its structure and properties. It states that Component B *is a parallel plate capacitor*, which is physically modeled with three layers as follows:



Write an expression for the capacitance of Component B as a function of dielectric permittivity ε and dimensions D_1, L, and W.

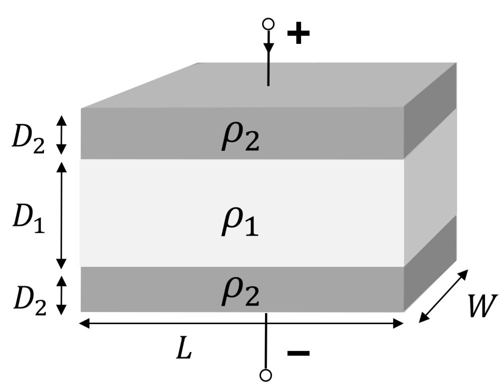
Solution:
The general capacitance of a parallel plate capacitor is

$$C = \varepsilon \frac{A}{d}$$

where ε is the permittivity of the material, A is the overlapping area of the parallel plates, and d is the separation distance of the parallel plates.
For this problem

$$C = \varepsilon \frac{A}{d} \quad \longrightarrow \quad C = \varepsilon \frac{L \cdot W}{D_1}$$

(c) (3 points) In the course of testing, your TA connected a large voltage source and put too much power through the capacitor. This resulted in the dielectric (the middle layer) breaking down, so that the entire three-layer device *behaves like a resistor*. After degradation, the device can be modeled as:



Write an expression for the *resistance* of Component B as a function of D_1, D_2, L, W, and resistivities ρ_1 and ρ_2.

Solution:

The general resistance of a resistor is

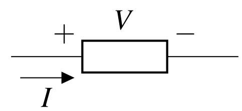
$$R = \rho \frac{l}{A}$$

where ρ is the resistivity of the material, l is the length of the resistor (in the direction of current flow), A is the cross-sectional area of the resistor (perpendicular to current flow).

For this problem we effectively have three resistors in series, since they share the same current.

$$R = R_1 + R_2 + R_3 = \rho_2 \frac{D_2}{L \cdot W} + \rho_1 \frac{D_1}{L \cdot W} + \rho_2 \frac{D_2}{L \cdot W} = \frac{2\rho_2 D_2 + \rho_1 D_1}{L \cdot W}$$

(d) (5 points) Your lab TA decides to try characterizing one final component and labels it 'Component C'. She connects Component C to a circuit and measures the voltage across it and current through it as shown



From her measurement she finds that $I = -5\,\mu\text{A}$ and $V = 0.2\,\text{V}$.

i. Is Component C labeled according to passive sign convention?

● Yes ○ No

Solution:
The current as labeled enters the positive voltage terminal (and exits the negative terminal), thus the voltage/current labeling adheres to passive sign convention.

ii. What is the power *dissipated* by Component C?

μW

Solution:
Component C is labeled according to passive sign convention, thus no sign adjustments to the power formula $P = V \cdot I$ are necessary and the result is the *dissipated power* whether positive or negative.

$$\begin{aligned} P = V \cdot I &= (0.2\,\text{V}) \cdot (-5\,\mu\text{A}) \\ &= -1\,\mu\text{W} \end{aligned}$$

The power dissipated by Component C is $P = -1\,\mu\text{W}$ (including the negative sign).

iii. Is Component C consuming or generating power?

○ Consuming ● Generating

Solution:
Component C is labeled according to passive sign convention and the computed power in part (d).ii. is negative, thus the element is *generating power*.

iv. Regardless of your answers to the previous parts, assume Component C generates a constant $10\,\mu\text{W}$ of power and is connected to a $1\,\text{mWh}$ battery (a 'Wh' or 'watt-hour' is a unit of energy). How long will it take to charge the battery from 0 to 100% capacity?

hours

Solution:

For constant power, the relationship between energy W and P over some time duration Δt is $W = P \cdot \Delta t$.

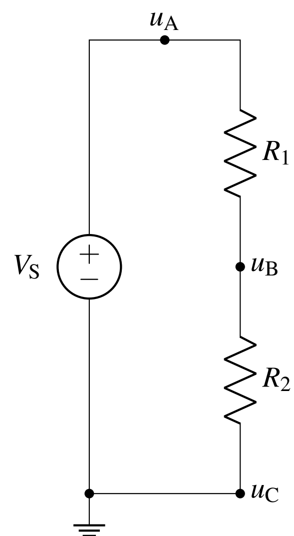
The battery requires $W = 1$ mWh of energy and is supplied by a constant $P = 10\,\mu\text{W}$ power source. Thus,

$$\Delta t = \frac{W}{P} = \frac{1\,\text{mWh}}{10\,\mu\text{W}} = \frac{1\,\text{mWh}}{0.01\,\text{mW}} = 100 \text{ hours}$$

3. Can You Divide a Divider? (16 Points)

For all parts please give your **answer in terms of the labeled circuit quantities**. When expressing your answers, you are free to use the parallel (||) operator.

(a) (4 points) Consider the circuit below.



i. Find the voltage at node u_B as a function of V_S, R_1, and R_2.

Solution: This circuit is a voltage divider. Referring to the voltage divider equation gives that

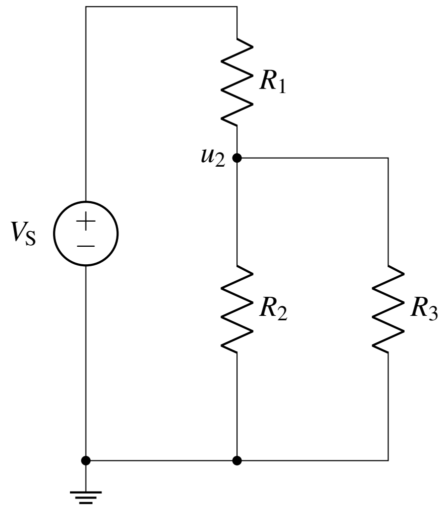
$$u_B = \frac{R_2}{R_1 + R_2} V_S$$

ii. How would you attach a voltmeter to check your answer for node voltage u_B? Indicate the **nodes** (i.e., u_A, u_B, or u_C) you would connect to each voltmeter terminal.

positive voltmeter terminal: $\boxed{}$ negative voltmeter terminal: $\boxed{}$

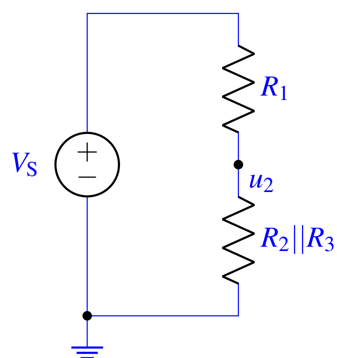
Solution:
Since u_C is ground, $u_C = 0\,\text{V}$. Then the voltage at u_B is just the voltage over R_2 since $u_B - u_C = u_B$. Thus to measure the voltage across R_2 we want to clip the voltmeter in parallel to R_2 with **Positive terminal: u_B, Negative terminal: u_C.**

(b) (4 points) Now consider a new circuit.



i. Find the voltage at node u_2 as a function of V_S, R_1, R_2, and R_3.

Solution:
Since we have an additional "load" resistor R_3, we can no longer directly apply the voltage divider equation. Instead we can first collapse parallel resistances R_2 and R_3 into an equivalent resistance $R_2||R_3 = \frac{R_2 R_3}{R_2+R_3}$. Then we have the following equivalent circuit:



We are left with a voltage divider and can once again apply the voltage divider equation

$$u_2 = \frac{R_2||R_3}{R_2||R_3 + R_1} = \frac{\frac{R_2 R_3}{R_2+R_3}}{\frac{R_2 R_3}{R_2+R_3} + R_1} V_S = \frac{R_2 R_3}{R_2 R_3 + R_1(R_2+R_3)} V_S$$

ii. How does the node voltage u_2 compare to the node voltage u_B in part (a)? Using 1-2 sentences, provide a conceptual reason for your answer.

○ $u_2 > u_B$ ○ $u_2 = u_B$ ● $u_2 < u_B$

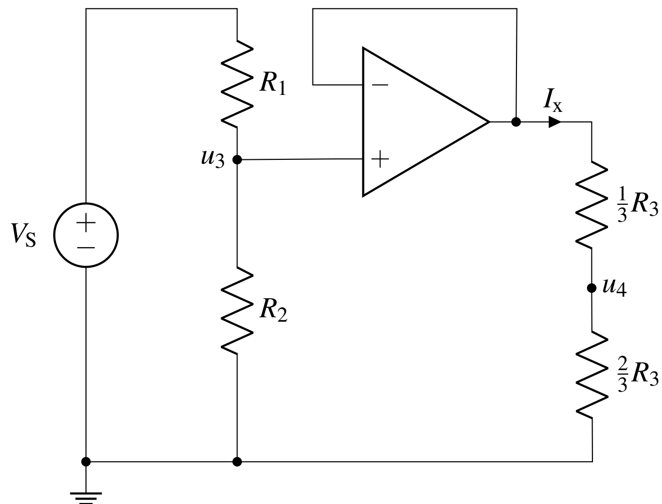
Solution:

For positive finite resistance values, the equivalent resistance $R_2||R_3$ must always be less than resistance R_2.

$$R_2||R_3 < R_2 \quad \longrightarrow \quad \frac{R_2R_3}{R_2+R_3} < R_2 \quad \longrightarrow \quad \frac{R_3}{R_2+R_3} < 1 \quad \checkmark$$

Consequently, the voltage at node u_2 is a smaller proportion of the applied voltage V_S than node voltage u_B in part (a), or $u_2 < u_B$.

(c) (8 points) Now consider a new circuit shown below. Assume the op-amp is ideal and in negative feedback.



i. Find an expression for the voltage at u_3 as a function of V_S, R_1, R_2, and R_3.

Solution:
From the Golden Rules we know that no current flows into either input terminal of the opamp, thus the first voltage divider is isolated from the rest of the circuit. As in part (a), we can use the voltage divider equation yielding

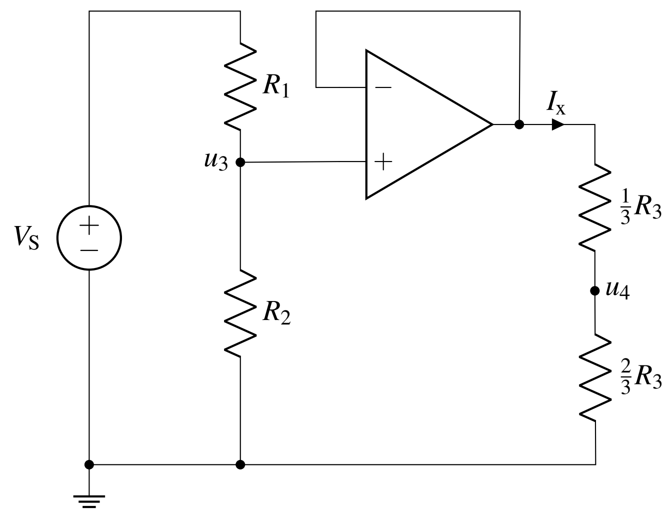
$$u_3 = \frac{R_2}{R_1 + R_2} V_S$$

which is an equivalent expression to the node voltage u_B in part (a).

ii. How does the node voltage u_3 compare to the node voltage u_2 in part (b)? Using 1-2 sentences, provide a conceptual reason for your answer.

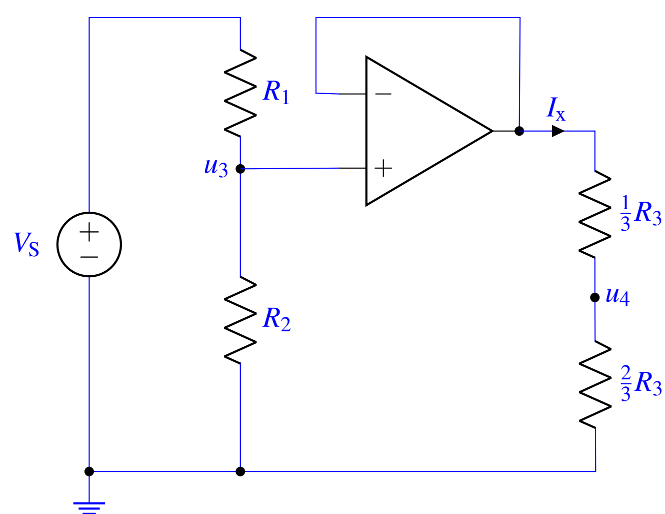
● $u_3 > u_2$ ○ $u_3 = u_2$ ○ $u_3 < u_2$

Solution:
By introducing the op-amp configured as a unity gain buffer, the two sub-circuits are isolated and prevented one from loading the other. Thus the node voltage u_3 should be identical to the node voltage u_B in part (a) and greater than the loaded node voltage u_2 in part (c), or $u_3 > u_2$.



iii. Find an expression for the voltage at u_4 as a function of V_S, R_1, R_2, and R_3. Your answer should NOT include any node voltages (i.e., u_3)

Solution:



The op-amp is in negative feedback, thus the second Golden Rule $u_+ = u_-$ can be applied and op-amp output voltage u_{out} is

$$u_{out} = u_- = u_+ = u_5 = \frac{R_2}{R_1 + R_2} V_S$$

From this, we see that u_6 is related to u_{out} via a voltage divider.

$$u_4 = \frac{\frac{2}{3}R_3}{\frac{1}{3}R_3 + \frac{2}{3}R_3} u_{out} = \frac{2}{3} u_{out}$$

Substituting the expression for u_{out} yields

$$u_4 = \frac{2}{3} u_{out} = \frac{2}{3} \cdot \frac{R_2}{R_1 + R_2} V_S = \frac{2R_2}{3(R_1 + R_2)} V_S$$

which is dividing the first divider from part (a)!!

iv. Find an expression for the current I_x as a function of V_S, R_1, R_2, and R_3. Your answer should NOT include any node voltages (i.e., u_3).

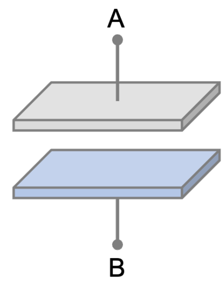
Solution:

$$I_x = \frac{u_3}{\frac{R_3}{2} + \frac{R_3}{2}} = \frac{R_2}{R_3(R_1 + R_2)} V_S$$

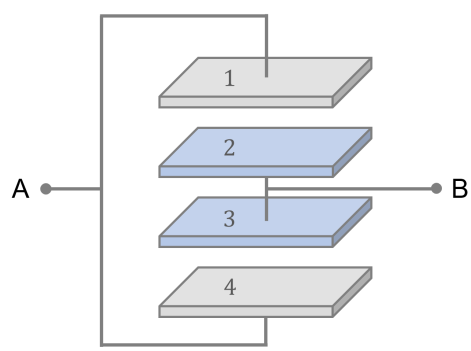
$$I_x = \frac{u_4}{\left(\frac{R_3}{2}\right)} = \frac{2}{R_3} \cdot \frac{R_2}{2(R_1 + R_2)} V_S = \frac{R_2}{R_3(R_1 + R_2)} V_S$$

4. Stacked Capacitors (11 points)

The parallel plate capacitor shown below is made up of two identical perfectly overlapping plates. The plates have length l, width w, are separated by distance d, and the dielectric material between the plates has permittivity ε. The capacitance formed by the two plates between nodes **A** and **B** is C_0.



(a) (3 points) Now assuming these same specifications, we stack 4 plates on top of each other. The plates are perfectly aligned vertically and the spacing between each plate is d. We connect node **A** to the top and bottom plates and node **B** to the middle two plates.



i. Is there capacitance formed between the 2nd and 3rd plates?

○ Yes ● No

Solution:
The 2nd and 3rd plates are connected to the same node, and thus always have the same voltage potential. Thus, no charge separation can form and there is no capacitance between them.

ii. Draw an equivalent capacitor circuit representing this physical arrangement of plates. Label nodes **A** and **B**.

Solution:
The top two plates form a capacitor C_1 between nodes **A** and **B**. Similarly, the bottom two plates also form a capacitor C_2 between nodes **A** and **B**. Note that the middle two plates do not form a capacitor since they are tied to the same node! Since C_1 and C_2 share the same nodes on both terminals, they are in parallel and we combine them into a single equivalent capacitor. Furthermore,

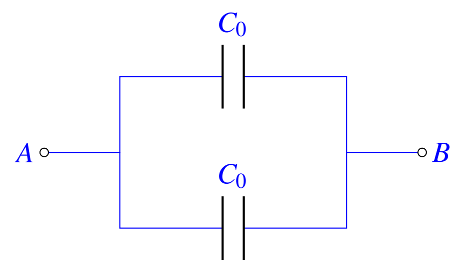
C_1 and C_2 have the same specifications as the capacitor in the problem statement so

$$C_1 = C_2 = C_0$$

and we can write

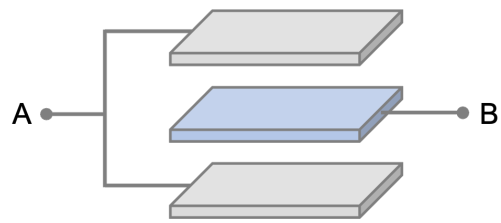
$$C_{\text{eq}} = C_1 + C_2 = 2C_0.$$

Full credit for the schematic with nodes A and B labeled. It is not necessary to identify the capacitance values.



(b) (2 points) From the capacitor configuration in part (a), we combine the two middle plates into a single plate. Assume all other specifications are the same as in part (a).

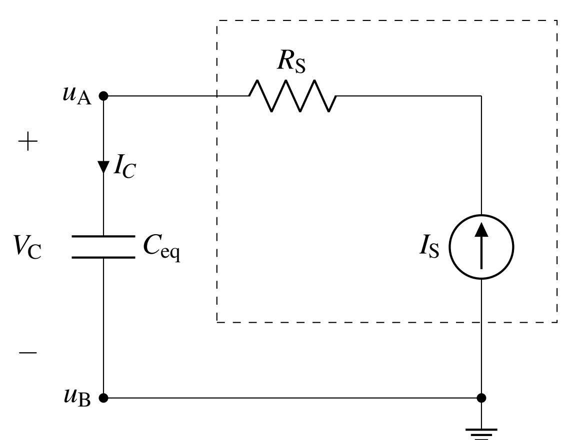
Find C_{eq}, the equivalent capacitance between nodes **A** and **B**. Express your answer in terms of C_0 (the equivalent capacitance of just two plates).



Solution:
This capacitor configuration is exactly the same as in part (a)! Even though the middle two plates were combined into one, the plate will still create a capacitor with both the top and bottom plate. This is similar to how the middle plate in the capacitive touchscreen also contributes to two differenct capacitors. However in contrast to the capacitive touchscreen example, the two capacitors formed here are in parallel since one node (**B**) is connected to the middle plate and one node (**A**) is connected to the top and bottom plates just like in the previous part. Thus we will again have

$$C_{\text{eq}} = C_1 + C_2 = C_0 + C_0 = 2C_0$$

(c) (6 points) We want to charge up our stacked capacitor, C_{eq}, with a current source. Unfortunately our current source is non-ideal, and instead can be modeled by an ideal current source, I_{S}, and a resistor, R_{S}, in series. The capacitor C_{eq} is uncharged at time $t = 0$.



i. Find an expression for the power dissipated by resistor R_{S} in terms of C_{eq}, I_{S}, R_{S}, and t.

Solution:
All elements have identical current I_{S} flowing through them which is invariant with time. In other words,

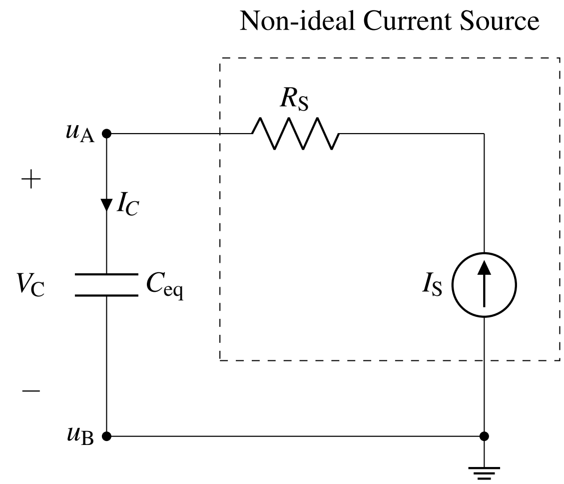
$$I_{C_{\text{eq}}}(t) = I_{\text{R}_{\text{S}}}(t) = I_{\text{S}}.$$

For the resistor, we can use Ohm's law to relate

$$V_{R_S}(t) = I_{R_S}(t)R_S.$$

Thus

$$P_{R_S}(t) = I_{R_S}(t)V_{R_S}(t) = I_{R_S}^2(t)R_S = I_S^2 R_S.$$



ii. Find the node voltage $u_A(t)$ in terms of C_{eq}, I_S, R_S, and t.

Solution: Since we have a single enclosed loop, the current supplied by the source I_S must flow through both the resistor R_S as well as the capacitor C_{eq}. Note that u_A represents the voltage drop across the capacitor so we know

$$Q = C_{eq} u_A. \tag{1}$$

In order to relate the charge on the capacitor Q with the current through the capacitor I_S, we note that

$$\frac{dQ}{dt} = I_S.$$

Taking the derivative of both sides of equation **??**, we see that

$$\frac{dQ}{dt} = I_S = C_{eq}\frac{du_A}{dt}.$$

Let's rearrange this equation and integrate:

$$\frac{du_A}{dt} = \frac{I_S}{C_{eq}}$$

$$du_A = \frac{I_S}{C_{eq}} dt$$

$$\int_{u_A(0)}^{u_A(t)} du_A = \frac{I_S}{C_{eq}} \int_{t=0}^{t=t} dt$$

$$u_A(t) - u_A(0) = \frac{I_S}{C_{eq}} t.$$

We are given the capacitor starts uncharged and so $u_A(0) = 0\,\text{V}$. Thus we have

$$u_A(t) = \frac{I_S}{C_{eq}} t.$$

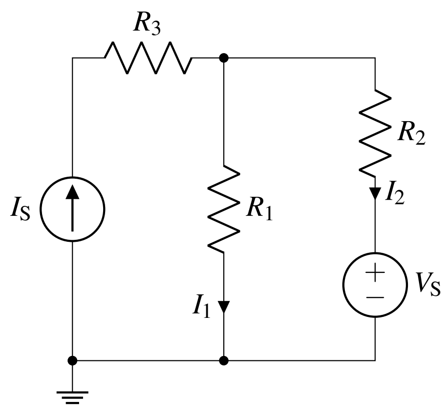
iii. Find an expression for the power delivered to the capacitor C_{eq} in terms of C_{eq}, I_{S}, R_{S}, and t. The capacitor voltage V_C and current I_C are labeled for you.

Solution:
Using the answers to parts (c).i. and (c).ii., we can write

$$P_{C_{\text{eq}}}(t) = I(t)V(t) = \frac{I_{\text{S}}^2}{C_{\text{eq}}}t.$$

5. A Plain Circuit (16 points)

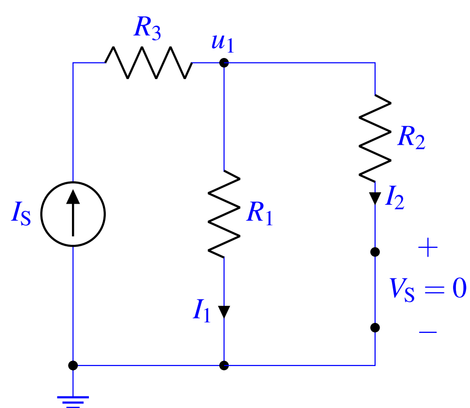
Consider the following circuit



(a) (3 points) Find the current I_1 passing through the resistor R_1 with the **current source turned on** and the **voltage source turned off**. Your answer must be *only* in terms of I_S, V_S, R_1, R_2, and R_3.

Solution:

When the voltage source is turned off (i.e., $V_S = 0$) it is an equivalent short circuit.



Method 1: Resistor Equivalence and Current Divider

The current I_S divides between the branches I_1 and I_2. The node voltage u_1 can be found using the equivalence of the parallel resistors R_1 and R_2.

$$u_1 = I_S \cdot (R_1||R_2)$$

The current I_1 through resistor R_1 is then

$$I_1 = \frac{u_1}{R_1} = \frac{I_S \cdot (R_1||R_2)}{R_1} = \frac{\left(\frac{R_1 R_2}{R_1+R_2}\right)}{R_1} I_S$$

$$I_1 = \frac{R_2}{R_1 + R_2} I_S$$

Method 2: Node Voltage Analysis

Alternatively, the node voltage u_1 can be found using node voltage analysis. First write a KCL equation at node u_1 as a function of the node voltages and resistances

$$I_S - I_1 - I_2 = 0$$
$$I_S - \frac{u_1 - 0}{R_1} - \frac{u_1 - 0}{R_2} = 0$$
$$R_1R_2I_S - R_2u_1 - R_1u_1 = 0 \quad \longrightarrow \quad u_1 = \frac{R_1R_2}{R_1+R_2}I_S$$

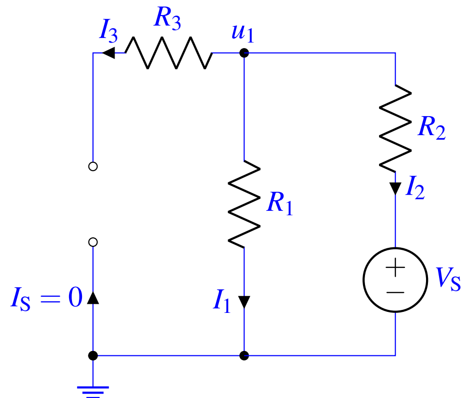
Finally using Ohm's Law, the current I_1 is related to the node voltage

$$I_1 = \frac{u_1}{R_1} = \frac{R_2}{R_1+R_2}I_S$$

(b) (3 points) Find the current I_1 passing through the resistor R_1 with the **current source turned off** and the **voltage source turned on**. Your answer must be *only* in terms of I_S, V_S, R_1, R_2, and R_3.

Solution:

When the current source is turned off (i.e., $I_S = 0$) it is an equivalent open circuit.



Method 1: Resistor Equivalence

No current flows through resistor R_3, thus it is equivalently a short circuit. Consequently, the two resistors R_1 and R_2 are in series. The loop current I_1 is then found by dividing the applied voltage V_S by the equivalent series resistance

$$I_1 = \frac{1}{R_1+R_2}V_S$$

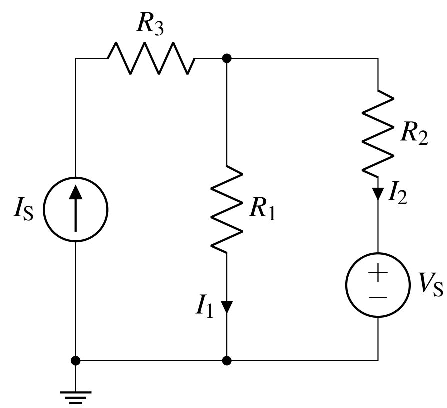
Method 2: Node Voltage Analysis

Alternatively, the node voltage u_1 can be found using node voltage analysis. First write a KCL equation at node u_1 as a function of the node voltages and resistances

$$I_1 + I_2 + I_3 = 0$$
$$\frac{u_1 - 0}{R_1} + \frac{u_1 - V_S}{R_2} - 0 = 0$$
$$R_2u_1 + R_1u_1 - R_1V_S = 0 \quad \longrightarrow \quad u_1 = \frac{R_1}{R_1+R_2}V_S$$

Finally using Ohm's Law, the current I_1 is related to the node voltage

$$I_1 = \frac{u_1}{R_1} = \frac{1}{R_1 + R_2} V_{\mathrm{S}}$$



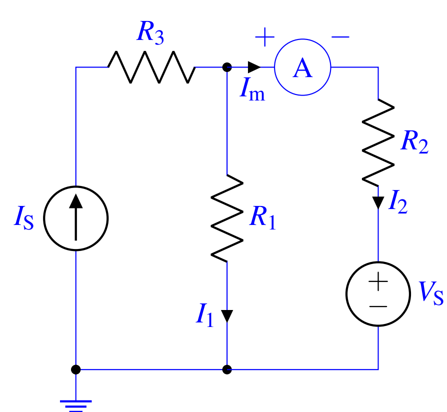
(c) (2 points) Using the principle of *superposition*, find the total current I_1 passing through the resistor R_1 when **both** the current source and voltage source are turned on. Your answer must be *only* in terms of I_S, V_S, R_1, R_2, and R_3.

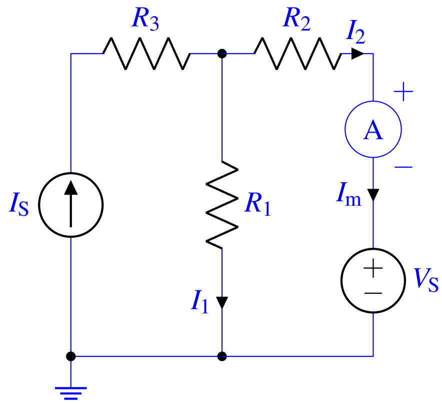
Solution:
Using the principle of superposition, we can sum the current I_1 through R_1 as a result of the voltage source, V_S, only and I_1 as a result of the current source, I_S, only. Thus we sum the solutions from part (a) and part (b)

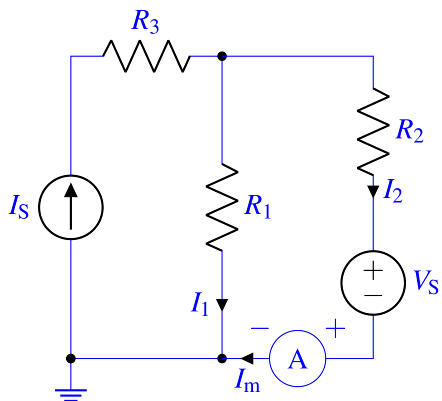
$$I_1 = I_1\Big|_{V_S=0} + I_1\Big|_{I_S=0}$$
$$I_1 = \frac{R_2}{R_1+R_2} I_S + \frac{1}{R_1+R_2} V_S$$

(d) (2 points) Redraw the circuit but with an ammeter added to measure the current I_2. Be sure to notate the direction of positive current for the ammeter.

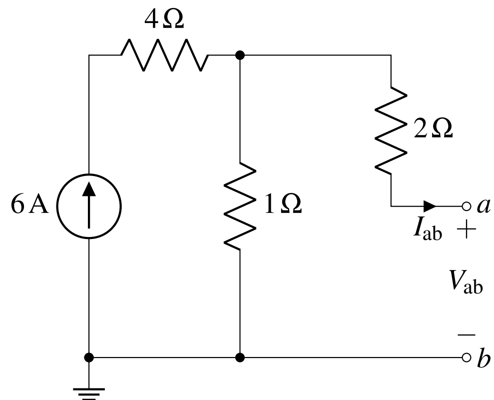
Solution:
Measuring current, I_m, with an ammeter requires breaking the circuit and placing the ammeter in series with the desired current. Three possible configurations are shown.



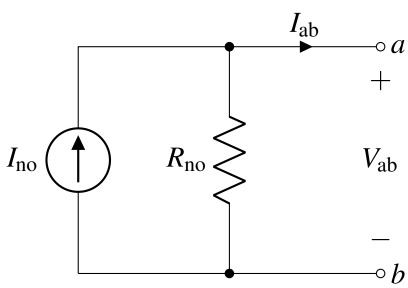

R_3
R_2
I_2
A
I_S
R_1
I_m
V_S
I_1


R_3
R_2
I_S
R_1
I_2
V_S
I_1
A
I_m

(e) (4 points) Now you want to determine the equivalent circuit seen from the voltage source V_S. You remove the voltage source from the circuit. You also now know the numerical values of the current source I_S and resistances R_1, R_2, and R_3.



For this circuit, derive the Norton equivalent between nodes a and b. Find the Norton current, I_{no}, and the Norton resistance, R_{no}.



I_{no} = $\boxed{}$ A

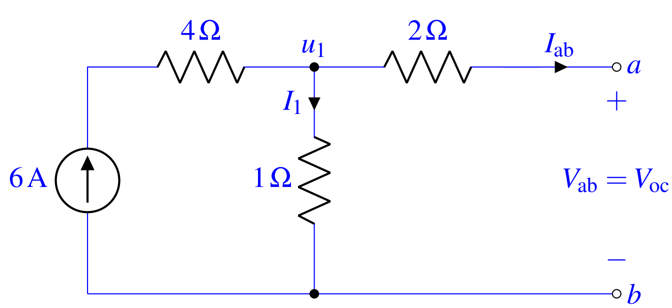
R_{no} = $\boxed{}$ Ω

Solution:

We need to derive two of the following three quantities: Thévenin voltage V_{th}, Norton current I_{no}, and Norton/Thévenin resistance $R_{no} = R_{th}$. Then these quantities can be related by $V_{th} = I_{no} \cdot R_{no}$ (derived from equivalence and Ohm's Law).

Open Circuit Test to Find $V_{th} = V_{oc}$

The open circuit test finds the voltage $V_{ab} = V_{oc}$ when an external open circuit is applied between nodes c and d. This is a useful test because the open circuit voltage and Thévenin voltage are equivalent (i.e., $V_{oc} = V_{th}$).



To find the open-circuit voltage V_{oc}, write a KCL equation at node u_1 and apply Ohm's Law to resistor

R_1

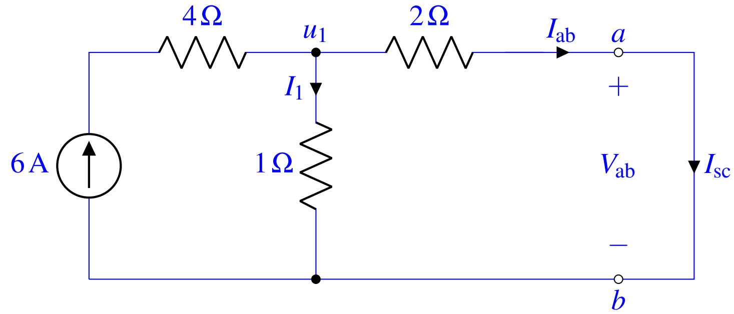
$$6\,\mathrm{A} - I_1 - I_{\mathrm{cd}} = 0$$
$$6\,\mathrm{A} - \frac{u_1}{1\,\Omega} - 0 = 0$$

Because $I_{\mathrm{ab}} = 0$, the node voltage u_1 is equivalent to V_{oc}

$$u_1 = 6\,\mathrm{V} = V_{\mathrm{oc}} = V_{\mathrm{th}}$$

Short Circuit Test to Find $I_{no} = I_{sc}$

The short circuit test finds the voltage $I_{\mathrm{ab}} = I_{\mathrm{sc}}$ when an external short circuit is applied between nodes *a* and *b*. This is a useful test because the short circuit current and Norton current are equivalent (i.e., $I_{\mathrm{sc}} = I_{\mathrm{no}}$).

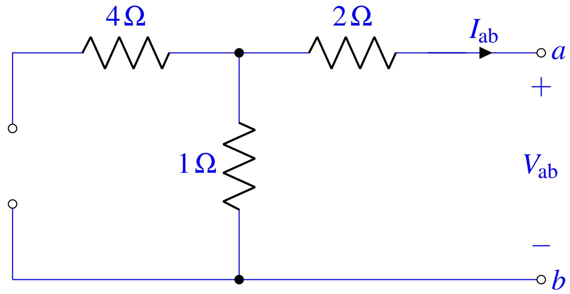


The short circuit current is same the current through the $2\,\Omega$ resistor which can be found using a current divider formula

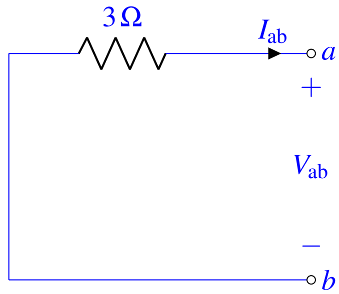
$$I_{\mathrm{sc}} = \frac{1\,\Omega}{2\,\Omega + 1\,\Omega} 6\,\mathrm{A} = 2\,\mathrm{A} = I_{\mathrm{no}}$$

Turn Off All Independent Sources to Find $R_{th} = R_{no}$

We can find the Thévenin/Norton resistance by turning off all independent voltage and current sources and deriving the equivalent resistance seen from terminals *a* and *b*.



Since the $4\,\Omega$ resistor has no current through it, it is an equivalent short circuit. Then the circuit reduces by combining the $1\,\Omega$ and $2\,\Omega$ resistors in series

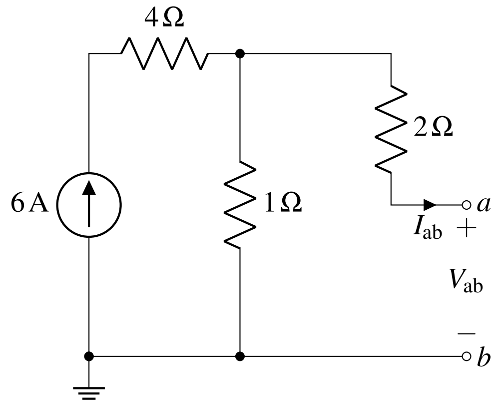


Thus the equivalent resistance between terminals a and b is

$$R_{ab} = 3\,\Omega = R_{th} = R_{no}$$

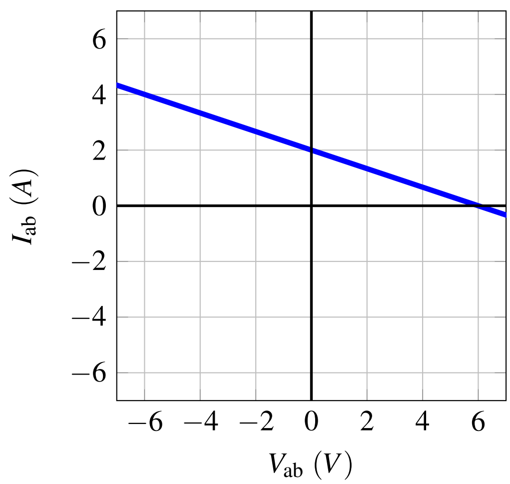
In summary,

$$\begin{aligned} V_{th} &= V_{oc} = 6\,\mathrm{V} \\ R_{th} &= R_{no} = 3\,\Omega \\ I_{no} &= I_{sc} = 2\,\mathrm{A} \end{aligned}$$

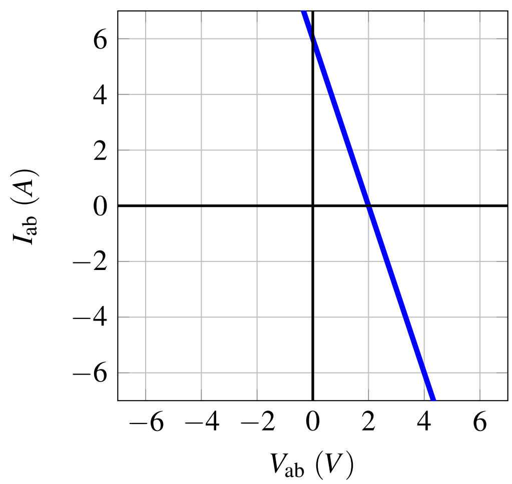


(f) (2 points) For the circuit in part (e), select the line which represents the I-V characteristic at terminals *a* and *b* (i.e., I_{ab} vs V_{ab})?

●



○



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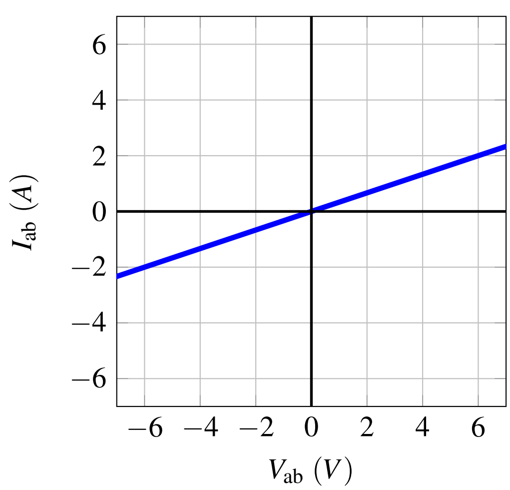

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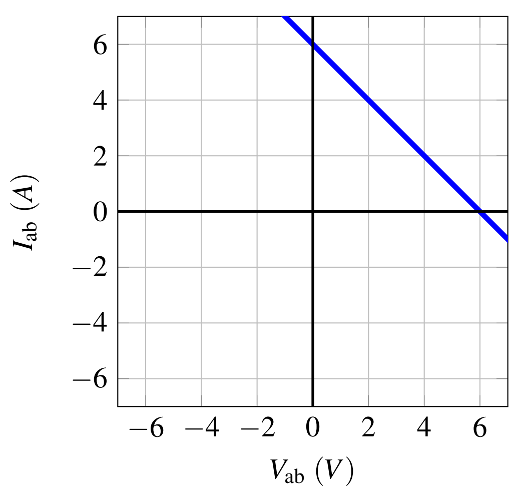


Solution:

To find the I-V characteristic at the terminals a and b, we must find the voltage and current with any two loads connected (e.g., short circuit, open circuit, load resistor).

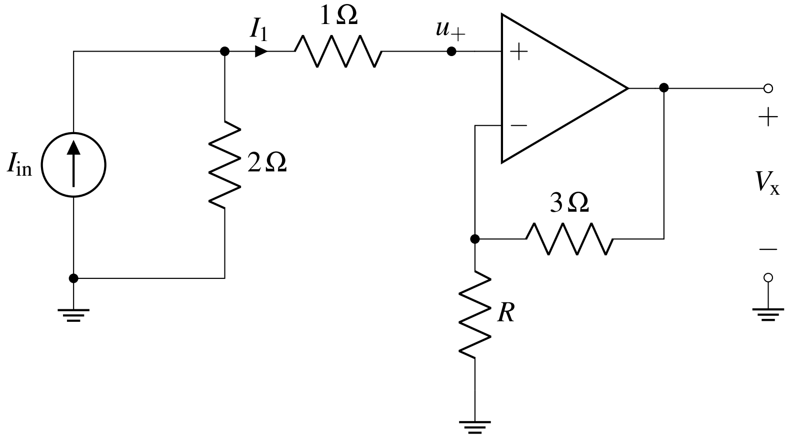
We can use the Norton equivalent circuit from part (e) since it has equivalent terminal characteristics to the full circuit. The simplest choices of load are when an open circuit is connected across a and b (i.e., $I_{\text{ab}} = 0$ and $V_{\text{ab}} = V_{\text{oc}} = V_{\text{th}} = 6\,\text{V}$) and when a short circuit is connected (i.e., $V_{\text{ab}} = 0$ and $I_{\text{ab}} = I_{\text{sc}} = I_{\text{no}} = 2\,\text{A}$).

Another option is to identify the slope of the I-V curve should be $-\frac{1}{R_{\text{no}}}$.

These two I-V operating points correspond to I-V curve #1.

6. Does The Circuit Blink? (17 points)

Consider the following circuit with an ideal op-amp



(a) (2 point) Is the op-amp configured in positive or negative feedback?

○ Positive feedback ● Negative feedback

Solution:
We will test for feedback by performing the wiggle test.
First, turn off the independent current source (equivalent open circuit). Next, increase (or wiggle) the op-amp output voltage, then the node voltage u_- will increase. This causes the expression $(u_+ - u_-)$ to decrease and thus the op-amp output voltage $V_x = A \cdot (u_+ - u_-)$ decreases.
We have shown that an increase in the op-amp output voltage causes a decrease in the same voltage. Thus, the op-amp is configured in *negative feedback*.

(b) (2 points) If $I_{in} = 1\,\text{A}$, then what is value of the current I_1?

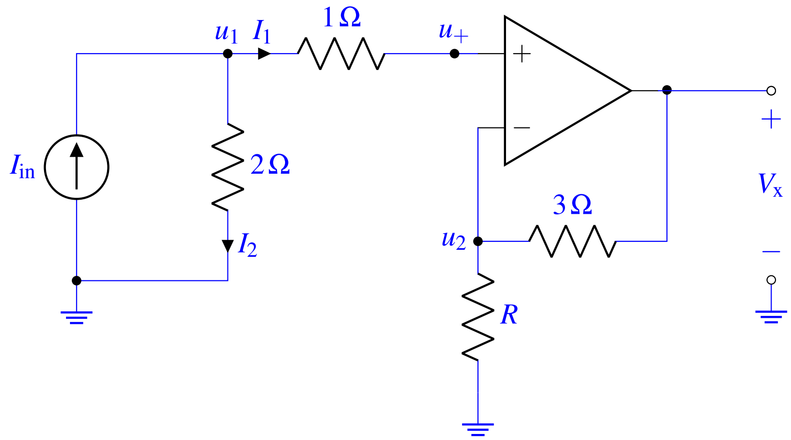
$I_1 =$ $\boxed{}$ A

Solution:
According to the Golden Rules of op-amps, the current into the input of the op-amp is $I_1 = 0\,\text{A}$. This current does not depend on the input current I_{in}.

(c) (2 points) If $I_{in} = 1\,\text{A}$, derive the voltage at node u_+.

$u_+ =$ $\boxed{}$ V

Solution:



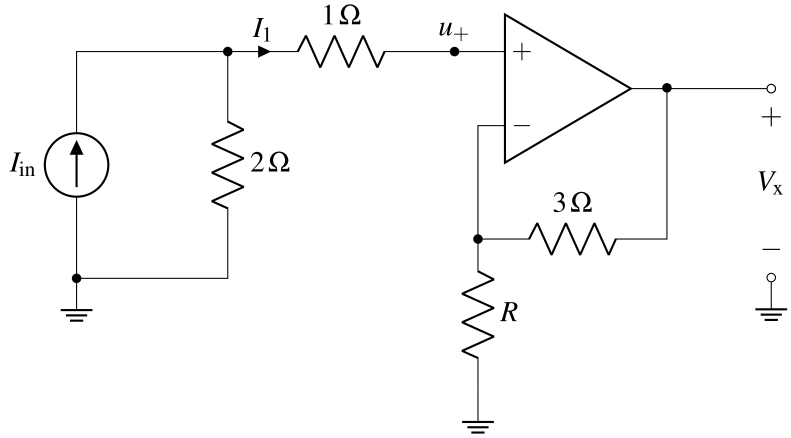
From the first Golden Rule we know that no current flows into either input terminal of the opamp, thus $I_1 = I_+ = 0$. Consequently, the current I_1 through the $1\,\Omega$ resistor is zero and the voltage at node u_1 and node u_+ are equivalent.

Writing KCL at the node u_1

$$I_{\text{in}} - I_1 - I_2 = 0$$
$$I_2 = I_{\text{in}} = 1\,\text{A}$$

and using Ohm's Law for the $2\,\Omega$ resistor

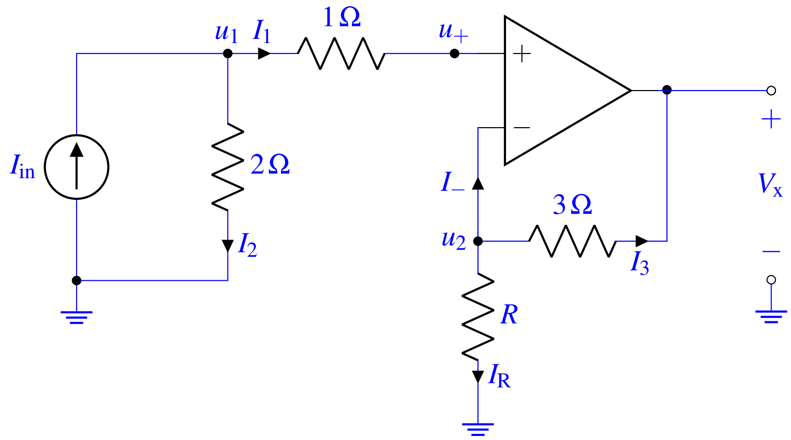
$$u_1 = I_2 \cdot (2\,\Omega) = (1\,\text{A})(2\,\Omega) = 2\,\text{V} = u_+$$



(d) (3 points) Determine the value of resistor R so that $V_{\text{x}} = I_{\text{in}} \cdot 5\,\Omega$.

$R =$ $\boxed{}$ Ω

Solution:



Now that the input current I_{in} is variable, we can rederive the voltage u_+ generally as

$$u_+ = u_1 = I_{\text{in}} \cdot 2\,\Omega$$

Since the op-amp is in negative feedback, we can apply the second Golden Rule: $u_+ = u_-$.

$$u_2 = u_- = u_+ = I_{\text{in}} \cdot 2\,\Omega$$

Thus we need a gain of $G = \frac{5}{2}$ from the op-amp circuit (to the right of the $1\,\Omega$ resistor) to boost I_{in} to $V_{\text{x}} = I_{\text{in}} \cdot 5\,\Omega$.

Method 1: Node Voltage

The op-amp input current I_- is zero by the first Golden Rule. Then we write a KCL equation at node

u_2

$$\begin{aligned} I_- + I_\mathrm{R} + I_3 &= 0 \\ I_\mathrm{R} + I_3 &= 0 \\ \frac{u_2 - 0}{R} + \frac{u_2 - V_x}{3\,\Omega} &= 0 \quad \longrightarrow \quad 3\,\Omega \cdot u_2 + Ru_2 - RV_x = 0 \end{aligned}$$

Solving this equation for V_x and substituting our earlier expression for u_2

$$V_\mathrm{x} = \frac{3\,\Omega + R}{R} u_2 = \frac{3\,\Omega + R}{R} \cdot (I_\mathrm{in} \cdot 2\,\Omega) = I_\mathrm{in} \cdot \left(\frac{3\,\Omega + R}{R} \cdot 2\,\Omega \right)$$

We want $V_\mathrm{x} = I_\mathrm{in} \cdot 5\,\Omega$

$$5\,\Omega = \frac{3\,\Omega + R}{R} \cdot 2\,\Omega \quad \longrightarrow \quad \frac{5}{2} = \frac{R + 3\,\Omega}{R} \quad \longrightarrow \quad \frac{5}{2} R = R + 3\,\Omega \quad \longrightarrow \quad \frac{3}{2} R = 3\,\Omega \quad \longrightarrow \quad R = 2\,\Omega$$

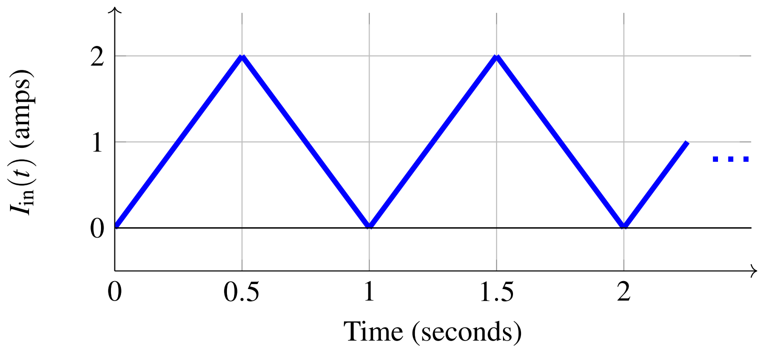
Method 2: Non-Inverting Op-Amp Gain

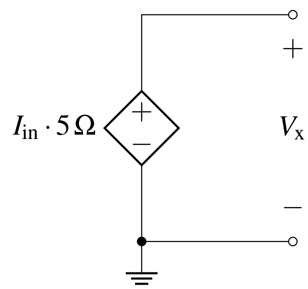
Alternatively, we can recognize the op-amp circuit is configured as a non-inverting amplifier and thus the desired gain (i.e., $\frac{5}{2}$) and resistance values can be related as

$$v_\mathrm{out} = G \cdot v_\mathrm{in} = \left(1 + \frac{3\,\Omega}{R} \right) v_\mathrm{in} = \frac{5}{2} v_\mathrm{in}$$

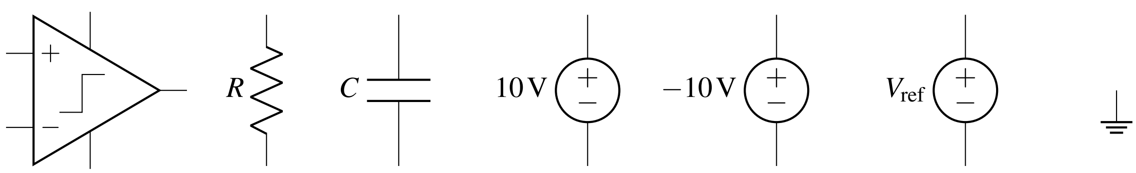
$$G = \frac{5}{2} = 1 + \frac{3\,\Omega}{R} \quad \longrightarrow \quad \frac{5}{2} = \frac{R + 3\,\Omega}{R} \quad \longrightarrow \quad \frac{5}{2} R = R + 3\,\Omega \quad \longrightarrow \quad \frac{3}{2} R = 3\,\Omega \quad \longrightarrow \quad R = 2\,\Omega$$

(e) (8 points) Now the input current $I_{\text{in}}(t)$ has the following triangular waveform with time. Regardless of your answer to the previous parts, assume you have successfully implemented the function of the circuit: $V_{\text{x}} = I_{\text{in}} \cdot 5\,\Omega$. Then the op-amp circuit can be represented with an equivalent circuit as shown.

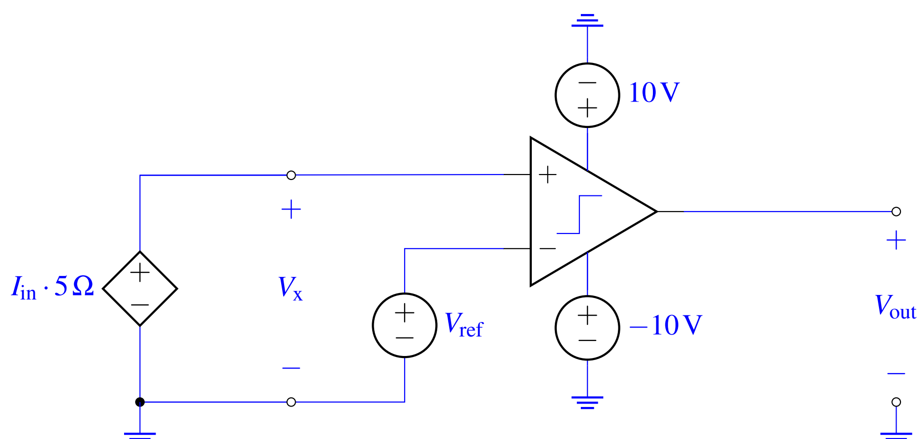




Using the voltage V_{x} as an input, design a comparator circuit that creates an output voltage $V_{\text{out}}(t)$ alternating periodically between a low voltage $-10\,\text{V}$ and high voltage $+10\,\text{V}$ with *equal durations*. You do not have to use every element and you can use multiple of each element. **If used, also specify your chosen values of R, C, and V_{ref} for each element.** Be sure to not leave any circuit element terminals unconnected.



Solution:



Other valid circuit solutions are possible. A non-comprehensive list includes swapping the connections to the $+$ and $-$ terminals of the comparator as well as creating a voltage reference using a resistive divider and the +10 V voltage source.

For the durations $t_{\text{high}} = t_{\text{low}}$, V_{ref} should be at the midpoint of the symmetrical triangular $V_{\text{x}}(t)$ waveform. The midpoint of the $V_{\text{x}}(t)$ is derived from the midpoint of the $I_{\text{in}}(t)$ waveform which is 1 A. Thus, the midpoint of $V_{\text{x}}(t)$ is 5 V which should be the value of V_{ref}.