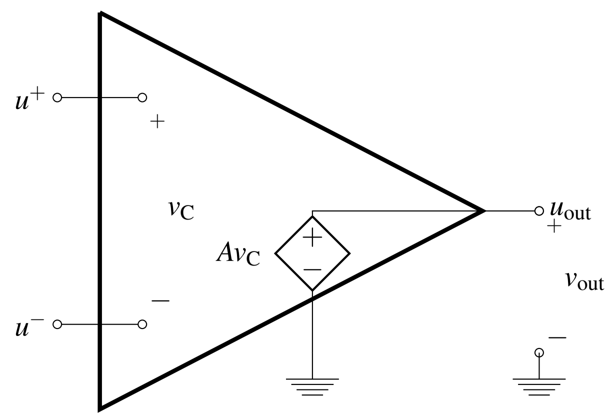
EECS 16A Designing Information Devices and Systems I
Spring 2019 Discussion 9A

1. Op-Amp Golden Rules

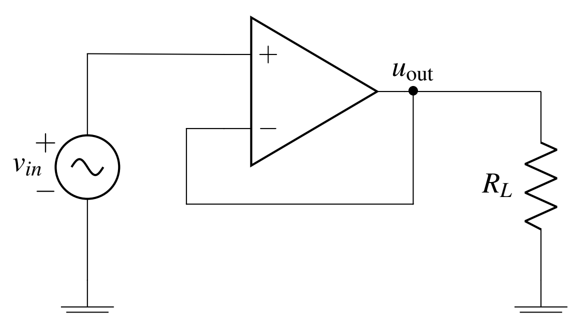
Here is an equivalent circuit of an op-amp (where we are assuming that $V_{SS} = -V_{DD}$) for reference:



(a) What are the currents flowing into the positive and negative terminals of the op-amp (i.e., what are I^+ and I^-)? What are some of the advantages of your answer with respect to using an op-amp in your circuit designs?

(b) Suppose we add a resistor of value R_L between u_{out} and ground. What is the value of v_{out}? Does your answer depend on R_L? In other words, how does R_L affect Av_C? What are the implications of this with respect to using op-amps in circuit design?

For the rest of the problem, consider the following op-amp circuit in negative feedback:



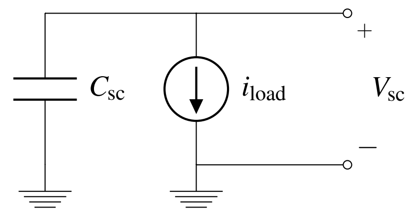
(c) Assuming that this is an ideal op-amp, what is v_{out}?

(d) Draw the equivalent circuit for this op-amp and calculate v_{out} in terms of A, v_{in}, and R_L for the circuit in negative feedback. Does v_{out} depend on R_L? What is v_{out} in the limit as $A \to \infty$?

2. IoT4eva Revisited

After guiding them to make an intelligent selection for their super-capacitors, IoT4eva was so happy with your performance that you got a promotion! The good news is that you're getting paid more, but the "bad" news is that you have more responsibilities too. In particular, you are now responsible not only for selecting the super-capacitors used to power the device, but also for building the rest of the circuitry associated with the power supply.

Recall that the super-capacitor supplies voltage and can be represented by the following circuit:



In practice, many real circuits (especially sensors that are trying to detect very small signals) don't like to operate with supply voltages that vary substantially over time. Remember that the voltage on our super capacitor drops linearly over time. If we want to use these super capacitors for our device, we need to build another circuit that converts this changing voltage into a constant voltage. This circuit is powered by the super-capacitor and produces a constant voltage at its output, which is then used to supply power to rest of the device. These circuits are often referred to as "voltage regulators," and in this problem we'll explore how to build the simplest form of such a voltage regulator.

(a) To create such a voltage regulator, we first need to build a reference voltage. The basic idea of the voltage regulator is that we will use V_{sc} to power an op-amp, and the op-amp will convert this reference voltage into our desired output voltage.

Fortunately, someone else in the company has already built one of those and made it available to you – the Thévenin equivalent of this circuit is a voltage source whose value is $0.8\,\text{V}$ and a resistance of $1\,\text{k}\Omega$. (The internals of this voltage reference circuit aren't important for this problem. Also, as you should see shortly, this circuit by itself is not appropriate for supplying power to the rest of the device.)

Using this reference circuit, an op-amp, and resistors, design a circuit that is powered by the super-capacitor voltage V_{sc} (which for now you can assume is always high enough for the circuit to work) that produces a constant $1.2\,\text{V}$ supply voltage for the rest of the device. You can model the load from the rest of the device as a $10\,\text{mA}$ current source. Please be sure to choose specific values for any resistors you use in your circuit as well.

Hint: Remember that the op-amp itself needs to be supplied with power, and the only source of power we have available is the super-capacitor.

(b) Now that we've built the voltage regulator and we know that we want its output voltage to stay fixed at $1.2\,\text{V}$, what is the minimum voltage we need on our super capacitors $V_{sc,min}$ to ensure that the regulator can indeed produce a fixed $1.2\,\text{V}$ output?

(c) One of the most important things to evaluate about a voltage regulator is its **efficiency**, or the power dissipated by the load circuits (in this case, the rest of the IoT4eva device) divided by the total amount of power delivered by the power supply. Continuing to model the rest of the IoT4eva device as a $10\,\text{mA}$ current source, how much power is dissipated by the $10\,\text{mA}$ current source?

Also, assuming that all of the IoT4eva's $10\,\text{mA}$ current flows through the super-capacitor, how much power is delivered by the super-capacitor? In this case, what is the overall efficiency of our design?