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EECS 16A    Designing Information Devices and Systems I  
Spring 2019    Homework 9

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**This homework is due April 5, 2019, at 23:59.**

**Self-grades are due April 9, 2019, at 23:59.**

**Submission Format**

Your homework submission should consist of **one** file.

- `hw9.pdf`: A single PDF file that contains all of your answers (any handwritten answers should be scanned).

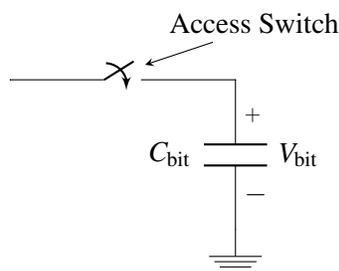
Submit the file to the appropriate assignment on Gradescope.

**1. Dynamic Random Access Memory (DRAM)**

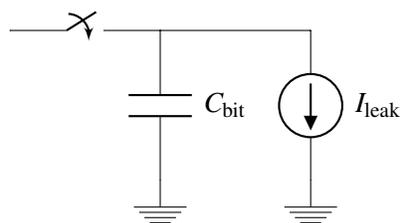
Nearly all devices that include some form of computational capability (phones, tablets, gaming consoles, laptops, ...) use a type of memory known as Dynamic Random Access Memory (DRAM). DRAM is where the “working set” of instructions and data for a processor is typically stored, and the ability to pack an ever increasing number of bits on to a DRAM chip at low cost has been critical to the continued growth in computational capability of our systems. For example, a single DRAM chip today can store  $> 8$  billion bits and is sold for  $\approx \$3$ - $\$5$ .

At the most basic level and as shown below, every bit of information that a DRAM can store is associated with a capacitor. The amount of charge stored on that capacitor (and correspondingly, the voltage across the capacitor) sets whether a “1” or a “0” is stored in that location.

Single DRAM Bit Cell



In any real capacitor, there is always a path for charge to “leak” off the capacitor and cause it to eventually discharge. In DRAMs, the dominant path for this leakage to happen is through the access switch, which we will model as a leakage to ground. The figure below shows a model of this leakage:



Fun Fact: This leakage is actually responsible for the “D” in “DRAM” – the memory is “dynamic” because after a cell is written by storing some charge onto its capacitor, if you leave the cell alone for too long, the value you wrote in will disappear because the charge on the capacitor leaked away.

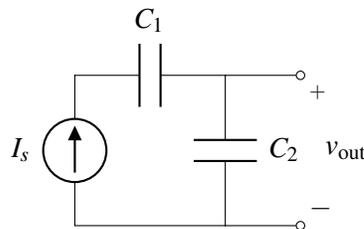
Let’s now try to use some representative numbers to compute how long a DRAM cell can hold its value before the information leaks away. Let  $C_{\text{bit}} = 28 \text{ fF}$  (note that  $1 \text{ fF} = 1 \times 10^{-15} \text{ F}$ ) and the capacitor be initially charged to  $1.2 \text{ V}$  to store a “1.”  $V_{\text{bit}}$  must be  $> 0.9 \text{ V}$  in order for the circuits outside of the column to properly read the bit stored in the cell as a “1.”

**What is the maximum value of  $I_{\text{leak}}$  that would allow the DRAM cell retain its value for  $> 1 \text{ ms}$ ?**

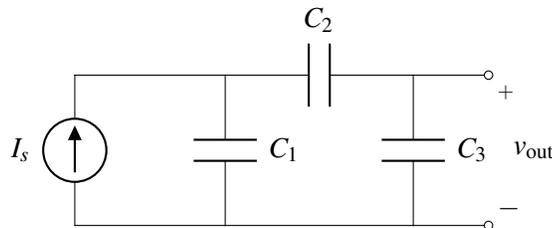
## 2. Current Sources And Capacitors

For the circuits given below, give an expression for  $v_{\text{out}}(t)$  in terms of  $I_s$ ,  $C_1$ ,  $C_2$ ,  $C_3$ , and  $t$ . Assume that all capacitors are initially uncharged, i.e. the initial voltage across each capacitor is  $0 \text{ V}$ .

(a)



(b)



## 3. Super-Capacitors

In order to enable small devices for the “Internet of Things” (IoT), many companies and researchers are currently exploring alternative means of storing and delivering electrical power to the electronics within these devices. One example of these are “super-capacitors” - the devices generally behave just like a “normal” capacitor but have been engineered to have extremely high values of capacitance relative to other devices that fit in to the same physical volume.

Your startup named **IoT4eva** is designing a new device that will revolutionize the process of making pizza, and you’ve been put in charge of selecting an energy source for it. You can’t find a battery that quite suits your needs, so you decide to try out some super capacitors in various configurations. The super capacitors will be charged up to a certain voltage in the factory and will then act as the power supply (source of voltage) for the electronics in your device.

(a) Assuming that your electronic device can be modeled as drawing a constant current source with a value of  $i_{\text{load}}$ , draw circuit models for your device using super-capacitors as the power supply with the following configurations:

- Config 1: a single super-capacitor as the power supply
  - Config 2: two super-capacitors stacked in series as the power supply
  - Config 3: two super-capacitors connected in parallel as the power supply
- (b) If each super-capacitor is charged to an initial voltage  $v_{\text{init}}$  and has a capacitance of  $C_{\text{sc}}$ , for each of the three configurations above, write an expression for the voltage supplied to your electronic device as a function of time after the device has been activated (i.e. connected to the super-capacitor(s)).
- (c) Now let's assume that your electronic device requires some minimum voltage  $v_{\text{min}}$  in order to function properly. For each of the three super-capacitor configurations, write an expression of the lifetime of the device.
- (d) Assume that a single super-capacitor doesn't provide you sufficient lifetime and so you have to spend the extra money (and device volume) for another super-capacitor. You consider the two following configurations:
- Config 2: two super-capacitors stacked in series
  - Config 3: two super-capacitors connected in parallel

When is Config 3 (parallel) better than Config 2 (series)? Your answer should involve conditions on  $v_{\text{init}}$  and  $v_{\text{min}}$ .

#### 4. Op-Amp in Negative Feedback

In this question, we are going to show that the second golden rule applies for op-amps in negative feedback. We will analyze circuits containing op-amps by first replacing the op-amp with our model, and then taking the limit as the open-loop gain ( $A$ ) approaches infinity.

Figure 1 shows the equivalent model of the op-amp. We can simplify further, by setting  $V_{DD} = -V_{SS}$  and assuming that the inputs ( $v_{in}$ ) are small enough for the output to not saturate to  $V_{DD}$  or  $V_{SS}$ . These assumptions result in the model in Figure 2 (Note 18, pg. 4).

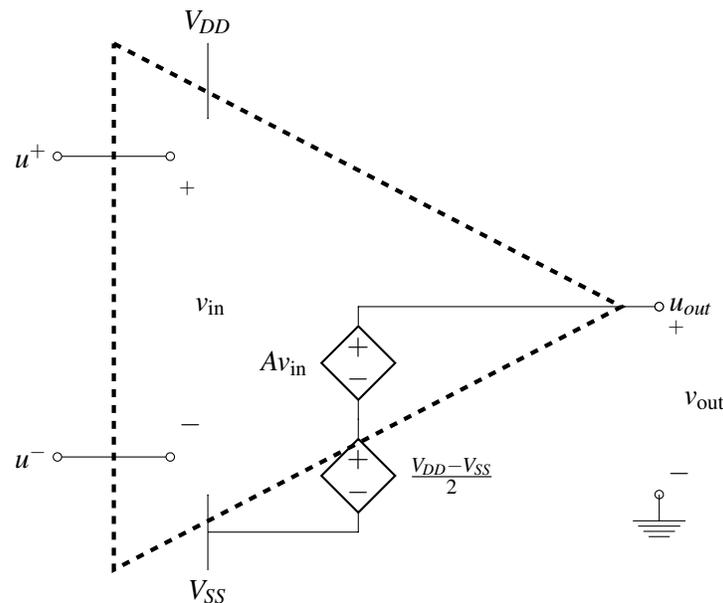


Figure 1: Op amp model

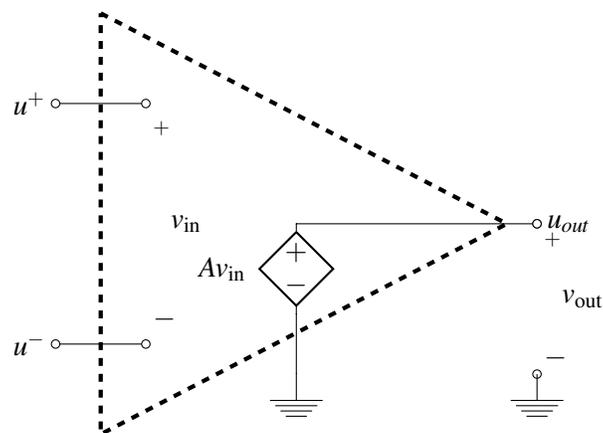
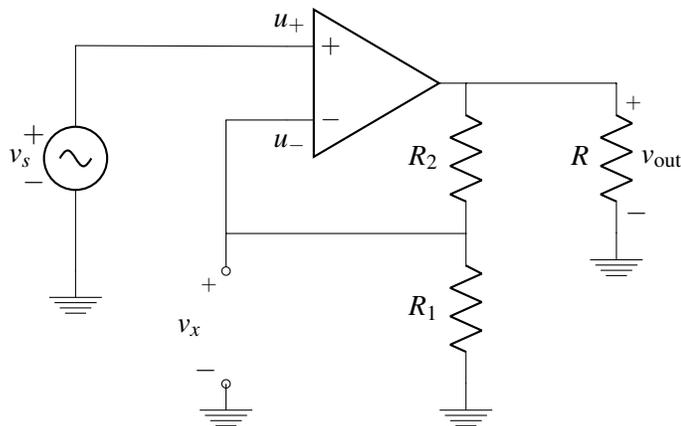


Figure 2: Op-amp model with the simplifying assumptions

(a) Now consider the circuit below.

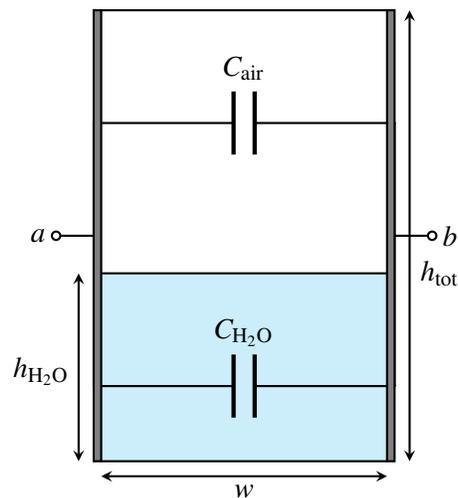
Draw an equivalent circuit by replacing the op-amp with the op-amp model shown above (Figure 2) and calculate  $v_{out}$  and  $v_x$  in terms of  $A$ ,  $v_s$ ,  $R_1$ ,  $R_2$  and  $R$ . Is the magnitude of  $v_x$  larger or smaller than the magnitude of  $v_s$ ? Do these values depend on  $R$ ?



(b) Using your solution to part (a), calculate the limits of  $v_{out}$  and  $v_x$  as  $A \rightarrow \infty$ . Do you get the same answers if you apply the fact that  $u_+ = u_-$  when there is negative feedback?

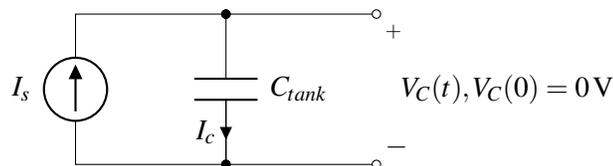
### 5. It's finally raining!

A lettuce farmer in Salinas Valley has grown tired of weather.com's imprecise rain measurements. Therefore, they decided to take matters into their own hands by building a rain sensor. They placed a rectangular tank outside and attached two metal plates to two opposite sides in an effort to make a capacitor whose capacitance varies with the amount of water inside.



The width and length of the tank are both  $w$  (i.e., the base is square) and the height of the tank is  $h_{\text{tot}}$ .

- What is the capacitance between terminals  $a$  and  $b$  when the tank is full? What about when it is empty?  
*Note:* the permittivity of air is  $\epsilon$ , and the permittivity of rainwater is  $81\epsilon$ .
- Suppose the height of the water in the tank is  $h_{\text{H}_2\text{O}}$ . Modeling the tank as a pair of capacitors in parallel, find the total capacitance between the two plates. Call this capacitance  $C_{\text{tank}}$ .
- After building this capacitor, the farmer consults the internet to assist them with a capacitance-measuring circuit. A fellow internet user recommends the following:



In this circuit,  $C_{\text{tank}}$  is the total tank capacitance that you calculated earlier.  $I_s$  is a known current supplied by a current source.

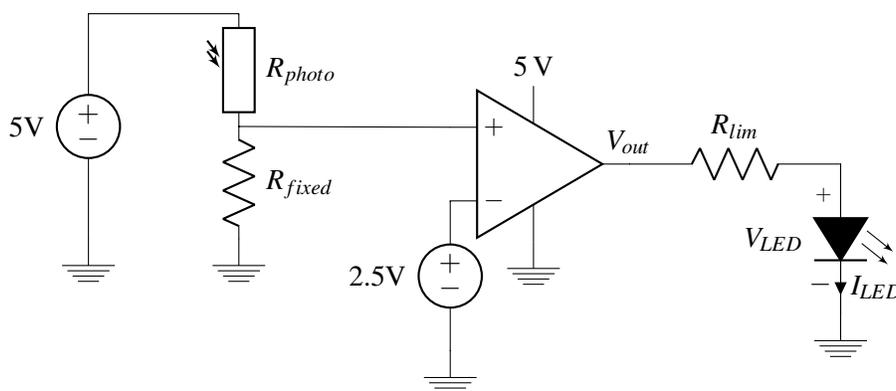
The suggestion is to measure  $V_C$  for a brief interval of time, and then use the difference to determine  $C_{\text{tank}}$ .

Determine  $V_C(t)$ , where  $t$  is the number of seconds elapsed since the start of the measurement. You should assume that before any measurements are taken, the voltage across  $C_{\text{tank}}$ , i.e.  $V_C$ , is initialized to  $0\text{ V}$ , i.e.  $V_C(0) = 0$ .

- Using the equation you derived for  $V_C(t)$ , describe how you can use this circuit to determine  $C_{\text{tank}}$  and  $h_{\text{H}_2\text{O}}$ .

## 6. LED Alarm Circuit

One day, you come back to your dorm to find that your favorite candy has been stolen. Determined to catch the perpetrator red-handed, you decide to put the candy inside a kitchen drawer. Using the following circuit design, you would like to turn on a light-emitting diode (LED) “alarm” if the kitchen drawer is opened.



Note  $R_{photo}$  is a photoresistor, which acts like a typical resistor but changes resistance based on the amount of light it is exposed to. This photoresistor is located inside the kitchen drawer, so we can tell when the drawer is opened or closed.

$V_{LED}$  indicates the voltage across the LED; we will guide you through the IV behavior of this element later in the problem. The LED is located in your room (and connected to a long wire going to the kitchen), so that you can remotely tell when the kitchen drawer has been opened.

- We see that the op-amp is in a comparator configuration. What is  $V_+$ , the voltage at the positive voltage input? Your answer should be written in terms of  $R_{photo}$  and  $R_{fixed}$ .
- We now want to choose a value for  $R_{fixed}$ . From the photoresistor's datasheet, we see the resistance in "light" conditions (i.e. drawer open) is  $1\text{ k}\Omega$ . In "dark" conditions (i.e. drawer closed), the resistance is  $10\text{ k}\Omega$ .

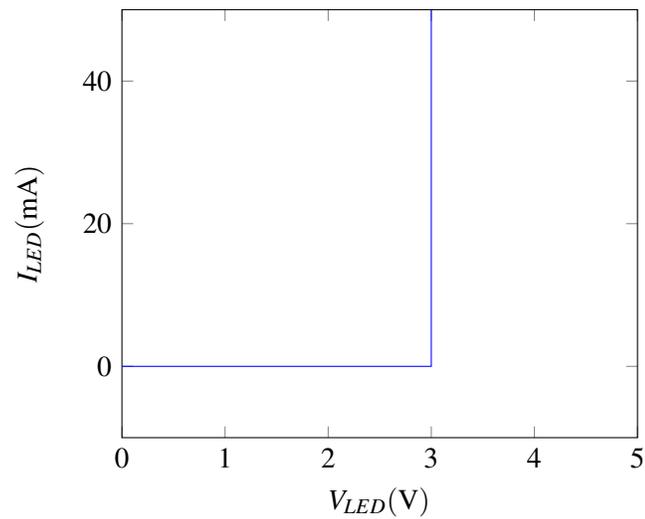
To ensure the comparator detects the light condition with more tolerance, we decide to design  $R_{fixed}$  so that  $V_+$  is  $3\text{ V}$  under the "light" condition. Solve for the value of  $R_{fixed}$  to meet this specification.

- Write down  $V_{out}$  with any conditions in terms of  $V_+$ . For simplicity, consider the case when  $V_+ \neq V_-$  and assume the op-amp is ideal.
- Using your answers to the previous parts, write down  $V_{out}$  with the conditions on its output in terms of  $R_{photo}$ . You can substitute the value of  $R_{fixed}$  you found in part (b). As before, you can assume that  $V_+ \neq V_-$  and the op-amp is ideal.
- From the design steps in the previous parts, we have designed a circuit that outputs non-zero voltage when the photoresistor is exposed to light (i.e. kitchen drawer open). We now want to design the LED portion of the circuit, so we get a visual alarm when the drawer is open.

From the LED's datasheet, the forward voltage,  $V_F$  is  $3\text{ V}$ . Essentially, if  $V_{LED}$  is less than this voltage, the LED won't light up and  $I_{LED}$  will be  $0\text{ A}$ .

Here is an idealized IV curve of this LED. The LED behaves in one of the following two modes:

- If the voltage across the LED is less than  $V_F = 3\text{ V}$  or if  $I_{LED} < 0\text{ A}$ , then the LED acts like an open circuit.
- If the voltage across the LED is  $V_F = 3\text{ V}$ , then the LED acts like a voltage source, except that it only allows positive current flow (i.e. only in the direction of current marked on the circuit diagram).



To avoid exceeding the power rating of the LED (and having it burn out), the recommended value for  $I_{LED}$  is 20 mA.

Find the value of the current-limiting resistor,  $R_{lim}$ , such that when the photoresistor is in the “light” condition,  $I_{LED} = 20$  mA.

### 7. Homework Process and Study Group

Who else did you work with on this homework? List names and student ID's. (In case of homework party, you can also just describe the group.) How did you work on this homework?