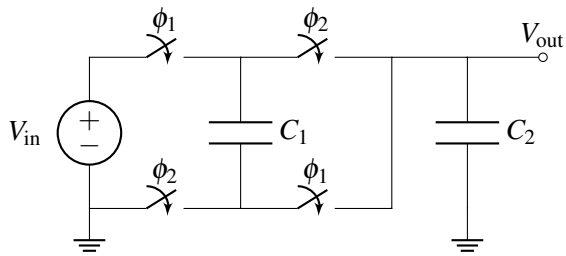
EECS 16A Designing Information Devices and Systems I
Spring 2021 Discussion 9A

1. Charge Sharing

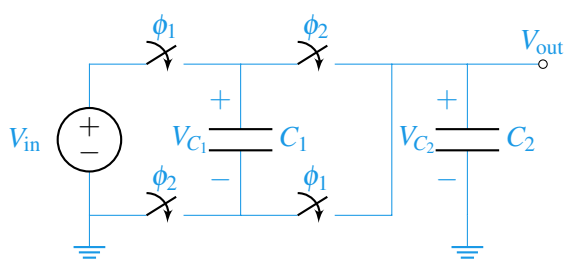
Consider the circuit shown below. In phase ϕ_1, the switches labeled ϕ_1 are on while the switches labeled ϕ_2 are off. In phase ϕ_2, the switches labeled ϕ_2 are on while the switches labeled ϕ_1 are off.



(a) Draw the polarity of the voltage (using + and − signs) across the two capacitors C_1 and C_2. (It doesn't matter which terminal you label + or −; just remember to keep these consistent through phase 1 and 2!)

Answer:

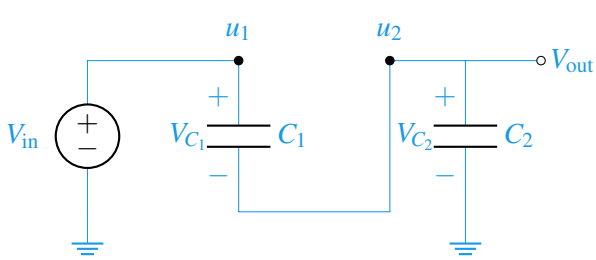
One way of marking the polarities is + on the top plate and − on the bottom plate of both C_1 and C_2. Let's call the voltage drop across C_1 V_{C_1} and across C_2 V_{C_2}.



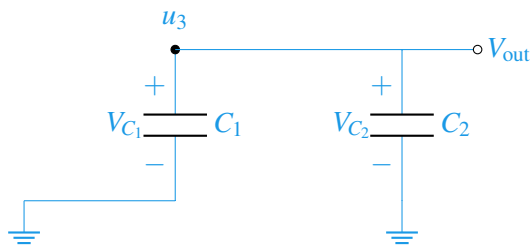
(b) Redraw the circuit in phase ϕ_1 and phase ϕ_2. Keep your polarity from part (a) in mind.

Answer:

Phase ϕ_1



Phase ϕ_2



(c) Find V_{out} in phase ϕ_2 as a function of V_{in}, C_1, and C_2.

Answer:

First, we must identify the floating node in phase ϕ_2. For this circuit, the floating node is u_3, as we can see that charge on the "+" plates of C_1 and C_2 cannot flow to ground.

Now that we know what plates are connected to our floating node, we must find the charge on those plates in phase ϕ_1. The two capacitors in series have a total capacitance of $C_{eq} = \frac{C_1C_2}{C_1+C_2}$. We know that there is a voltage of V_{in} across this capacitor and thus $Q_{C_{eq}} = V_{\text{in}}\frac{C_1C_2}{C_1+C_2}$ charge. Because they're in series, we know that the charge across the equivalent capacitance is the same as a charge across each individual capacitor. Since we are looking for the charge on the "+" terminals of those capacitors it will be:

$$\begin{aligned} Q_{u_3}^{\phi_1} &= Q_{C_1} + Q_{C_2} \\ &= 2Q_{C_{eq}} \\ &= 2V_{\text{in}}\frac{C_1C_2}{C_1+C_2} \end{aligned}$$

Similarly, we must find the charge on those plates in phase ϕ_2.

$$\begin{aligned} Q_{u_3}^{\phi_2} &= V_{C_1}C_1 + V_{C_2}C_2 \\ &= (u_3 - 0)C_1 + (u_3 - 0)C_2 \\ &= (V_{\text{out}} - 0)C_1 + (V_{\text{out}} - 0)C_2 \\ &= V_{\text{out}}(C_1 + C_2) \end{aligned}$$

Because of the conservation of charge, we can equate the total charge in phase ϕ_1 and phase ϕ_2.

$$\begin{aligned} Q_{u_3}^{\phi_1} &= Q_{u_3}^{\phi_2} \\ 2V_{\text{in}}\frac{C_1C_2}{C_1+C_2} &= V_{\text{out}}(C_1+C_2) \\ V_{\text{out}} &= 2\frac{C_1C_2}{(C_1+C_2)^2}V_{\text{in}} \end{aligned}$$

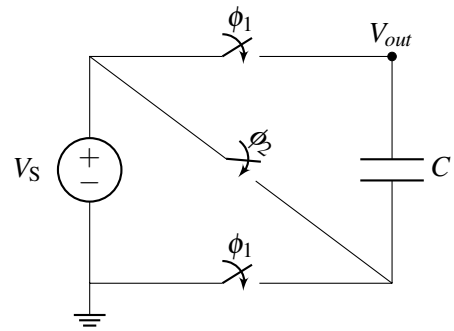
(d) How will the charges be distributed in phase ϕ_2 if we assume $C_1 \gg C_2$?

Answer:

We know that the capacitors are in parallel in phase ϕ_2, so the voltage across both capacitors is the same. Considering that $Q = CV$, if $C_1 \gg C_2$, then $Q_1 \gg Q_2$.

2. Voltage Booster

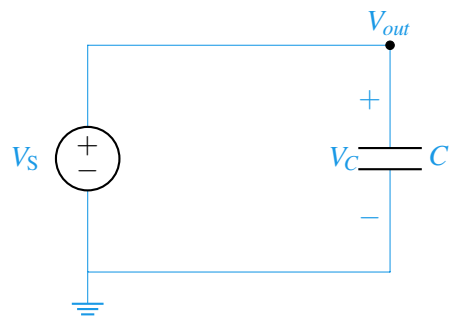
We have made extensive use of resistive voltage dividers to reduce voltage. What about a circuit that boosts voltage to a value greater than the supply $V_S = 5V$? We can do this with capacitors!



(a) In the circuit above switches ϕ_1 are initially closed and switch ϕ_2 is initially open. Calculate the value of the output voltage, V_{out} with respect to ground, and the amount of charge stored on capacitor, C, at that state (phase 1).

Answer:

In this setting we have the following equivalent circuit:



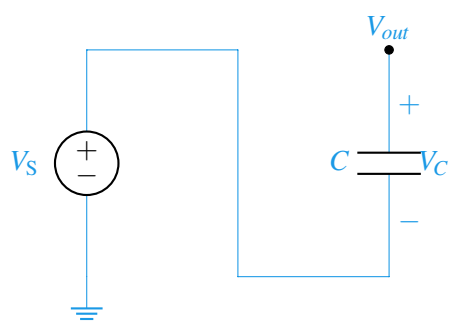
Hence,

$$V_{out} = V_S, \quad Q = CV_S.$$

(b) Now, after the capacitors are charged, switches ϕ_1 are opened and switch ϕ_2 is closed. Calculate the new voltage output voltage, V_{out}, at steady state.

Answer:

Phase 2 equivalent ckt:



In phase 2 notice that the voltage source is connected to the *negative* plate of capacitor C, while the positive plate is left floating (since it is open). Hence, charge is going to be conserved on the top plate

of C. However, in phase 2: $V_C^{\phi_2} = V_{out} - V_S$:

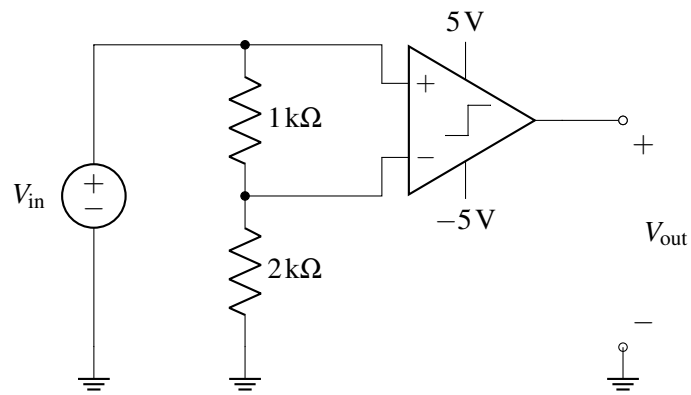
$$Q_C^{\phi_1} = Q_C^{\phi_2} \Rightarrow CV_S = C(V_{out} - V_S) \Rightarrow V_out = 2V_S = 10V!$$

We have created a voltage doubler!

3. Comparators

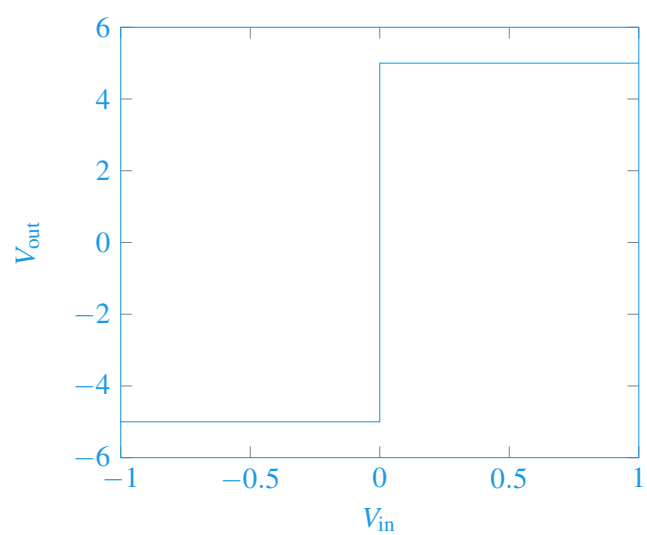
For each of the circuits shown below, plot V_{out} for V_{in} ranging from $-10\,\text{V}$ to $10\,\text{V}$ for part (a) and from $0\,\text{V}$ to $10\,\text{V}$ for part (b).

(a)

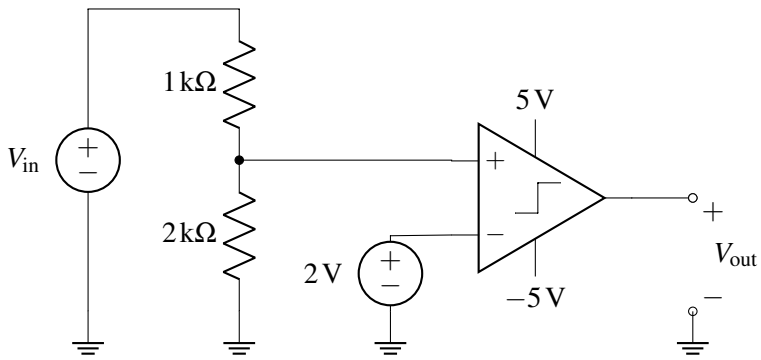


Answer:

When the positive terminal's voltage, V_+, is greater than the negative terminal's voltage, V_-, the value at the positive supply rail, V_{DD},will be output. Likewise, if the negative terminal's voltage, V_-, has a higher voltage then the value at the negative supply rail, V_{SS}, will be output. Since V_- is just the output of a voltage divider with the source $V_{\text{in}} = V_+$, it will always have lower absolute value and same polarity as the positive terminal. Thus, the comparator's output will depend only on the sign of the source V_{in}.

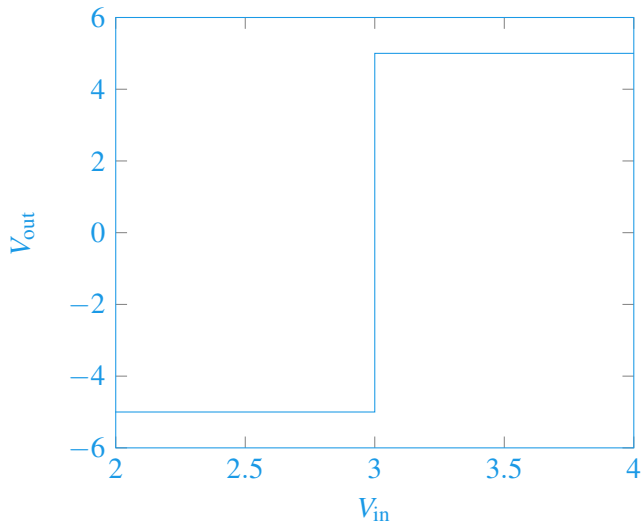


(b)



Answer:

$$V_+ = \frac{2\,\text{k}\Omega}{1\,\text{k}\Omega + 2\,\text{k}\Omega} V_{in} = \frac{2}{3} V_{in}$$

$$V_- = 2\,\text{V}$$

The comparator will output positive 5V when the voltage divider's output $V_+ > 2\,\text{V}$ and thus when $V_{in} > 3\,\text{V}$. Otherwise, it will output -5V.