EECS16A DIS4D

* Don't forget: Discussion checkoff form today (#10)

Today's topics

[1] Op amps: What are they and what do they do?

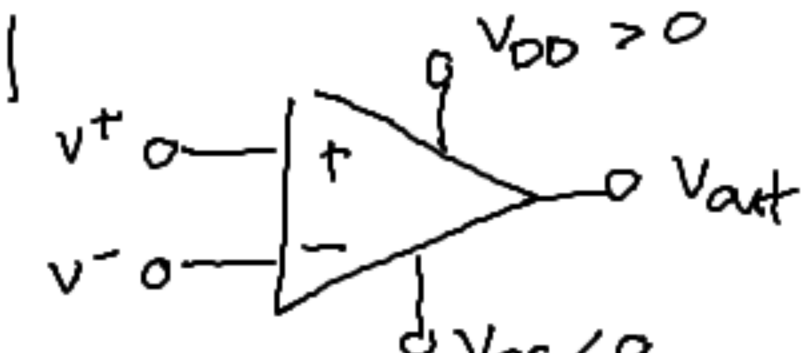
[2] Introduction to the inverting amplifier (and also, buffer)

Op. amp: Operational Amplifier

Operational → Mathematical operations

Amplifier → circuit element that amplifies voltages & currents

Symbol



V_{DD} & V_{SS} are sources/power supplies

→ • Addition and subtraction of voltages

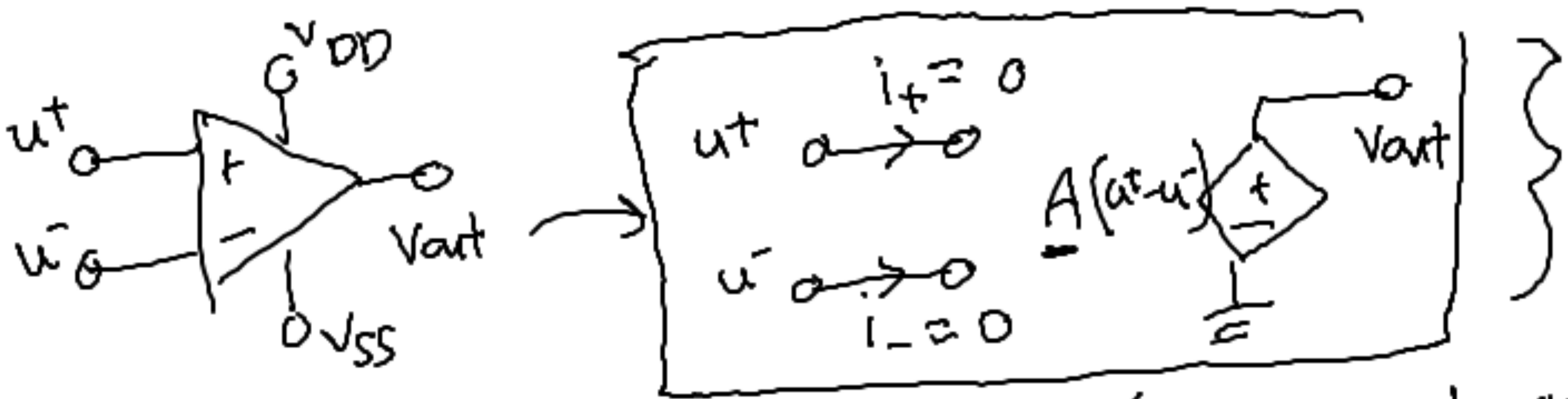
• Integration & differentiation " "

→ • Multiply a voltage by a constant (amplification when multiplier > 1)

→ • Linear combination of voltages

• Multiplication of voltages (nonlinear)

↳ out of scope/ not in focus



} model for what's inside an ideal op amp

1. G.R. #1 : Currents going into +/- terminals are zero
2. G.R. #2 : $v^+ = v^-$ if NFB, $A = \infty$ (ideal)

$V_{out} = A(v^+ - v^-)$

$A = \infty$

$V_{out} = V_{DD} \geq 0$ if the value of $A(v^+ - v^-)$ is too high

$V_{out} = V_{SS} \leq 0$ if the value of $A(v^+ - v^-)$ is too low

(Def) Gain : the scaling factor of an input voltage (quantity) to an output voltage (quantity)

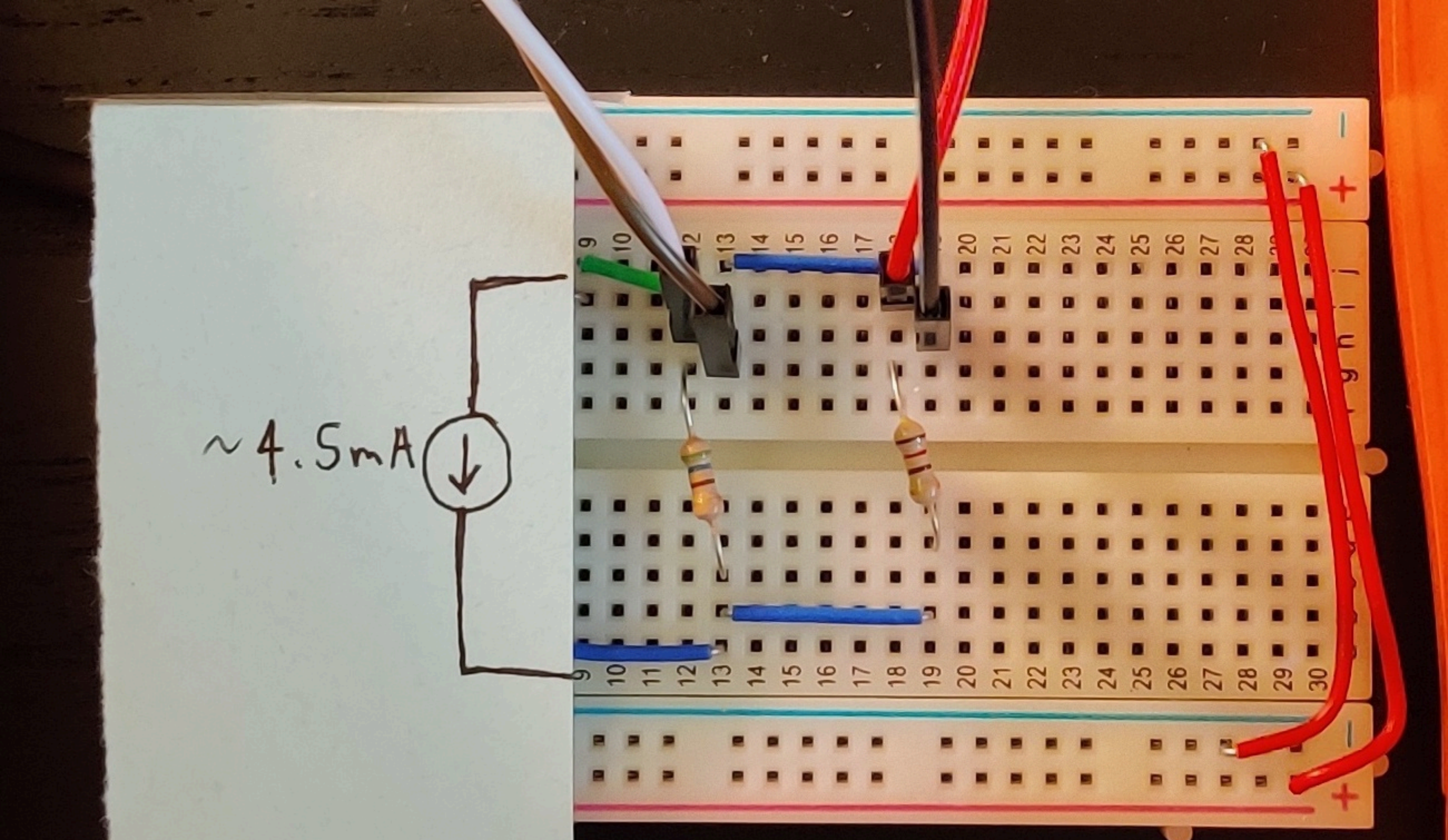
output voltage → $V_{out} = A(v^+ - v^-)$ ← "input voltage"

A ← gain of an op amp (without FB)

A_v ← gain of an op amp ckt w/ FB

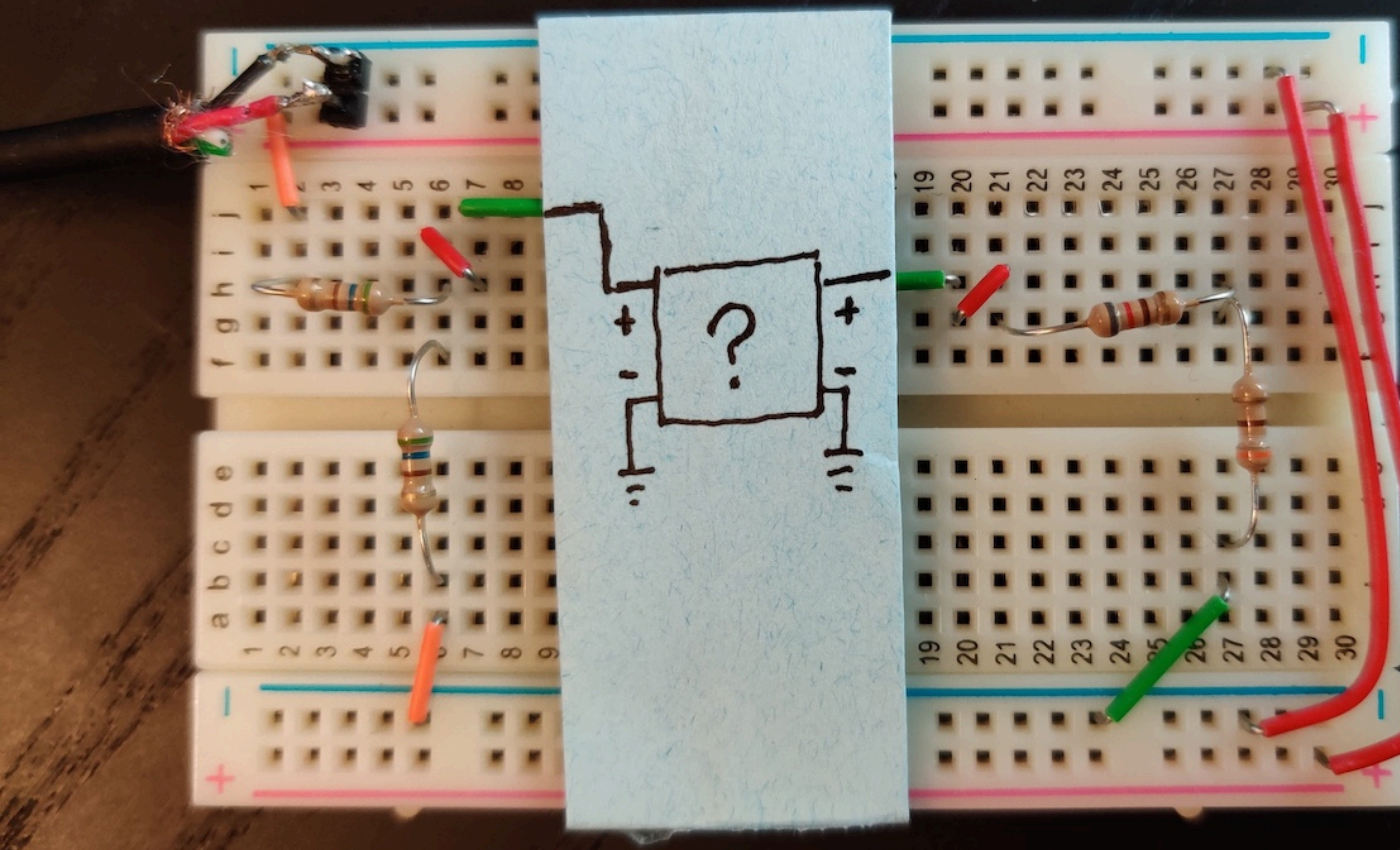
In DIS 3C : Saw that sticking two voltage dividers together did not behave how we wanted (loading)

Loading : the phenomenon where a voltage in a circuit changes due to connecting another ckt on its output



Current divider demo from DIS3B with current divider implemented with "magic element"

Circuit from DIS3C Extra Demo with “magic element”

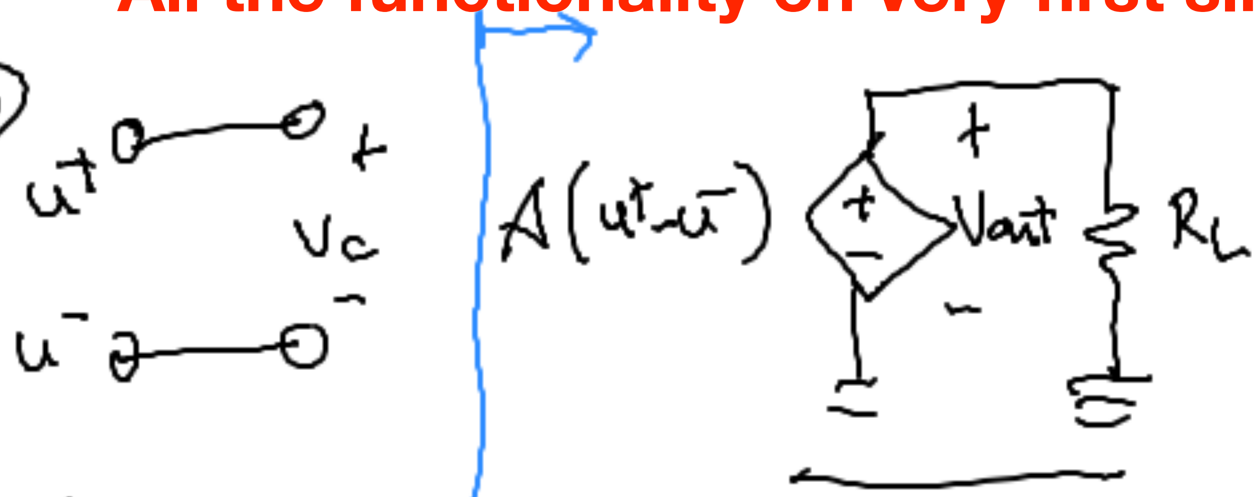


Benefit of op amps (magical!)

- Solves loading problem (DIS 3C Q2)
- Build a current source

*All the functionality on very first slide

1 (b)



$V_{out} = ?$

$= AV_c$

$= A(u^+ - u^-)$

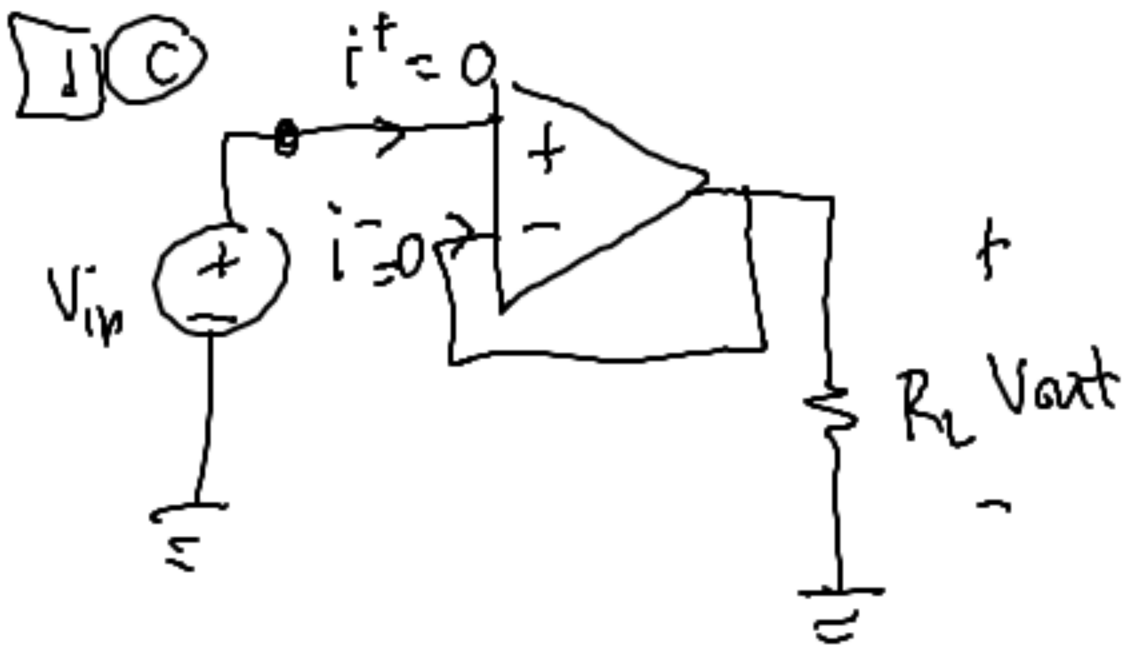
$R_L = 100\,\Omega$ $\quad$ $R_L = 10\,k\Omega$

$V_{out} = AV_c$ $\quad$ $V_{out} = AV_c$

why the same?: R_L is in parallel w/ AV_c,

$V_{out} = AV_c$ only dependent on u^+, u^-

1 (c)



Let's apply GR

1. $i^+ = i^- = 0$

[$u^+ = V_{in}$] → Not a GR

2. If NFB, $u^+ = u^-$. Check ✓

Check NFB

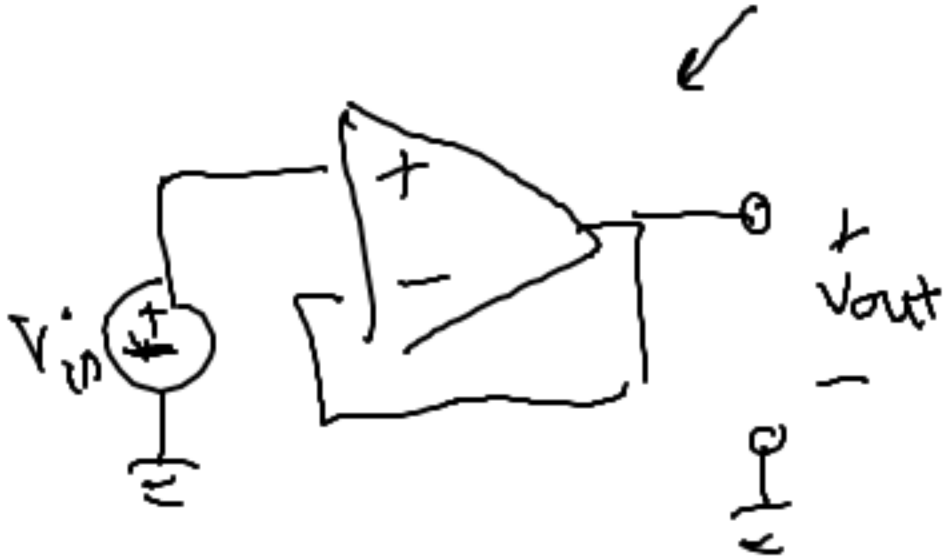
2 (a) Turn off sources

2 (b)

u^- node voltage increases (same node)

$V_{out} = A(u^+ - u^-)$
↓ dec. $\quad$ ↑ inc.

Conclusion:
$V_{in} = u^+ = u^- = V_{out}$



This circuit takes V_{in} and makes $\boxed{V_{out} = V_{in}}$

Unity gain buffer ↳ thing that goes in between circuits, helps connect/moderate

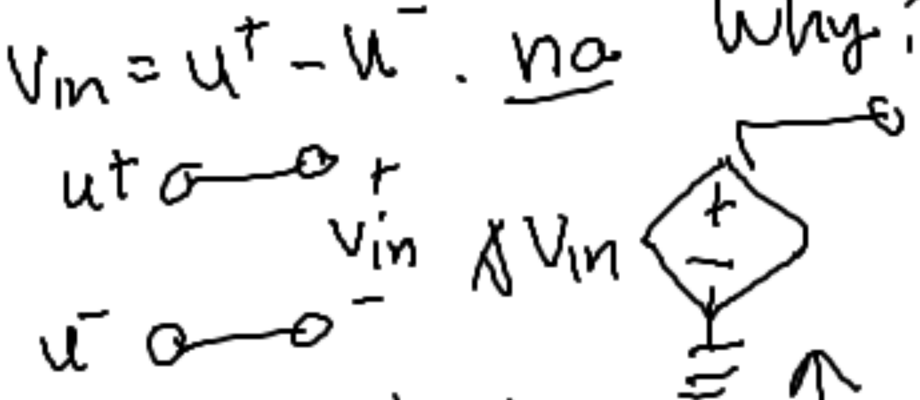
"1" $A_v =$ multiplier for feedback

$$V_{out} = A_v V_{in}$$

$$\frac{V_{out}}{V_{in}} = A_v = 1$$

Memorize the block above

Q: Is $V_{in} = u^+ - u^-$. no Why?



Shown in lecture

V_{in} never refers to source on (+) terminal

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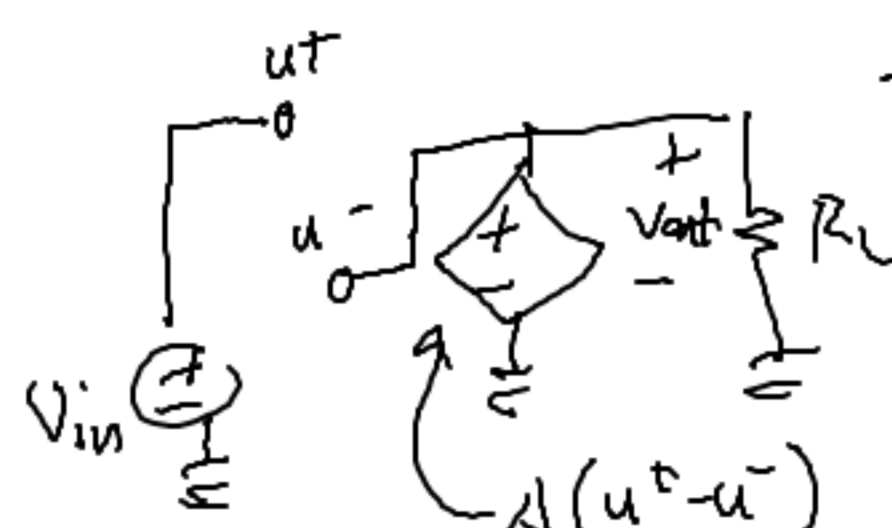
1 (d) In ideal case R_L does not make V_{out} change.



$\rightarrow V_{out} = A(u^+ - u^-)$

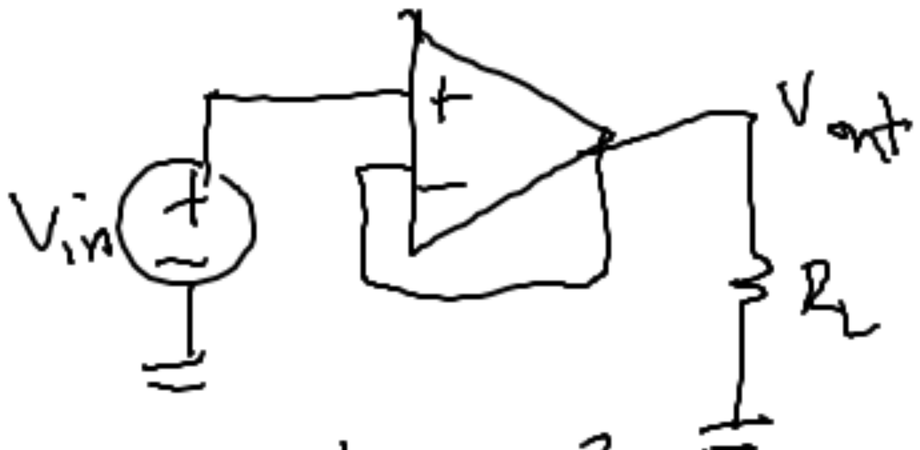
$V_{out} = A(V_{in} - V_{out})$

$V_{out} + AV_{out} = AV_{in}$

$V_{out} = \frac{A}{1+A} V_{in}$

$A \rightarrow \infty \quad V_{out} = V_{in}$

When A is not infinite R_L still doesn't affect V_{out}



Q: What's I_{R_L}?
when $A = \infty$

$$V_{out} = V_{in}$$

$$I_{R_L} = \frac{V_{out}}{R_L} \neq 0$$

when $A \neq \infty$

$$V_{out} = \frac{A}{1+A} V_{in}$$

$$I_{R_L} = \frac{V_{out}}{R_L} \neq 0$$

2 Inverting Amplifier

Derive Vout as a function of Vin (Use NVA)

Don't choose to write KCL @ output be

ⓐ u^- KCL: $I_1 = i^- + I_2$

$I_1 = I_2$ (GR#1)

why 0?
$u^- = u^+ = 0V$
NFB
(GR#2)

$$\frac{0 - V_{in}}{R_1} = \frac{V_{out} - 0}{R_2}$$

$$\boxed{V_{out} = -\frac{R_2}{R_1} V_{in}}$$

$$A_v = -\frac{R_2}{R_1} \quad \text{(negative)}$$

↖ gain w/ FB

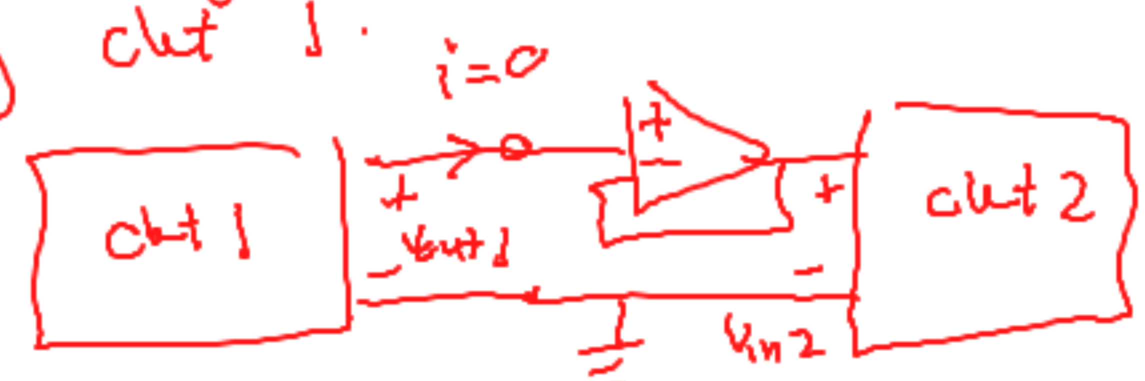
Extra Notes / Questions

URL for circuit sim of inverting amplifier: tinyurl.com/y45fb625

Q: Does the unity gain buffer use an ideal op amp?
↳ We'll assume op amps are ideal in this course, so yes.

Q: Are A_v and A different?
↳ Yes. A_v - gain $\left(\frac{V_{out}}{V_{in}}\right)$ with feedback (determined by ckt around op amp)
A - gain $\left(\frac{V_{out}}{V_{in}}\right)$ without feedback (intrinsic to op amp)

Q: What's the purpose of the unity gain buffer?
↳ Prevents loading, let's us connect ckt 1 to ckt 2 without affecting ckt 1.



$V_{out1} = V_{in2}$