Module 2, Lecture 10

EECS 16A
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* Troll problem w/ Op-Amps } Note 19
* Cascading Ckt Blocks

* Cascading + Composing Ckt Blocks (Cont.) } Note 20
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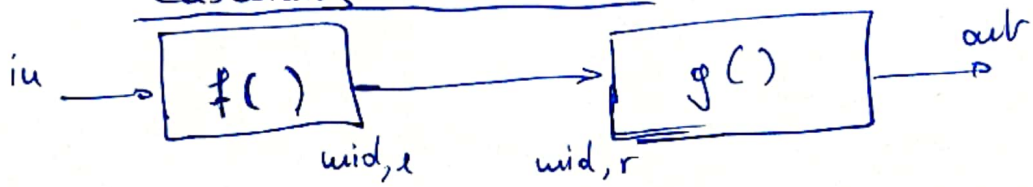
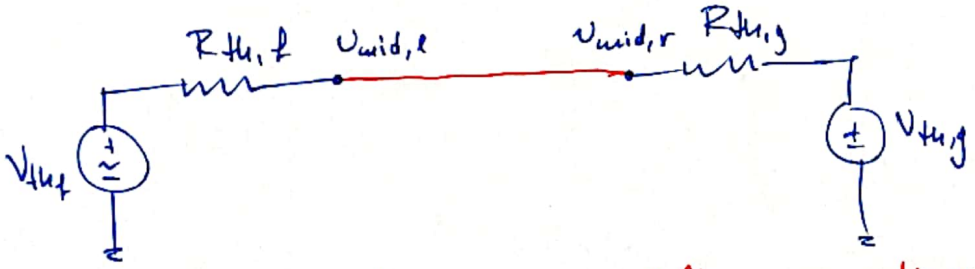
* Design Examples

Cascading Ckt Blocks





(most likely zero since we are looking at the in of block g( ))

Before connection: $v_{mid,l} = V_{th,f}$

After connection:

$$v_{mid,l} = v_{mid,r} = \frac{R_{th,g}}{R_{th,g}+R_{th,f}} V_{th,f} + \frac{R_{th,f}}{R_{th,g}+R_{th,f}} V_{th,g}$$

$\neq$ in general

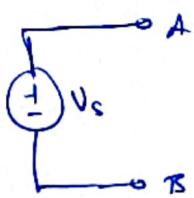
$\therefore$ except when: $R_{th,f} = 0$ (wire)

or $R_{th,g} = \infty$ (open-circuit)

Ideal Isolation

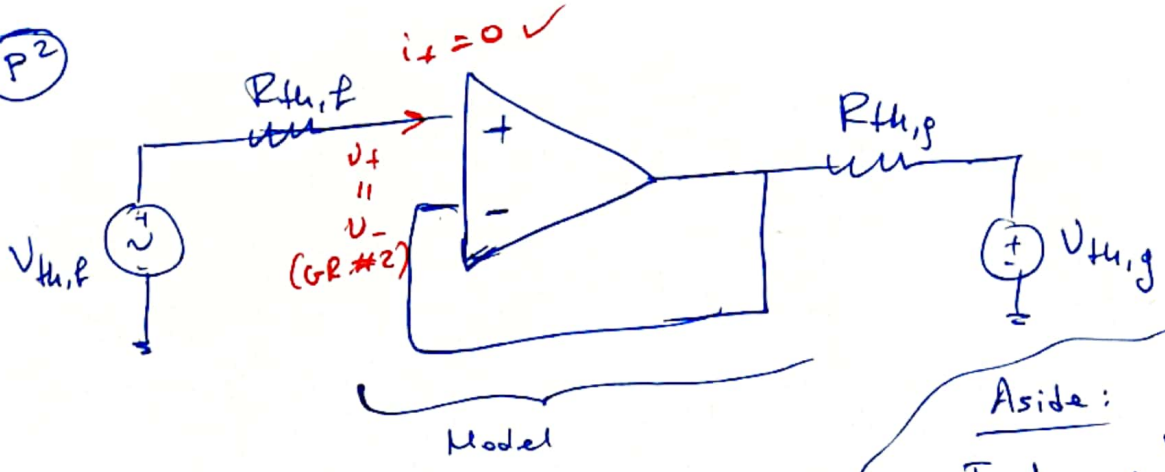
From the perspective of block f: see an open-circuit $R_{th,g} = \infty$

—"— —"— "— g: see a voltage source $R_{th,f} =$

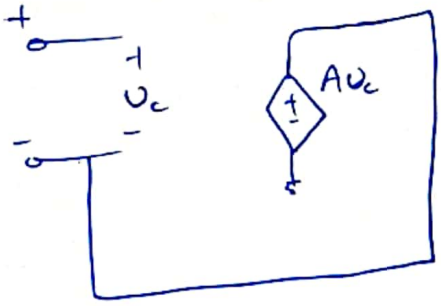


R_{th}, Volt source $= 0$

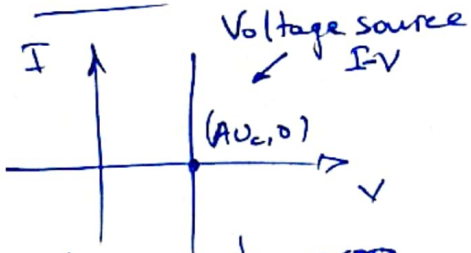
P2



Model



Aside:



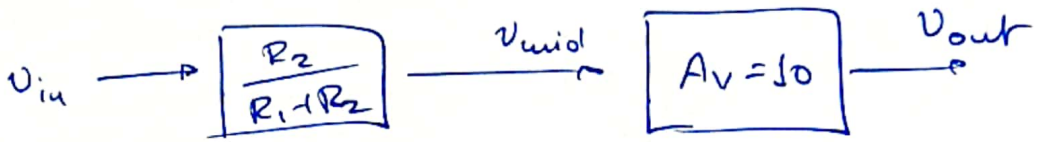
slope $= \frac{1}{R} = \infty$

$\Rightarrow R = 0$

Aside 2: for current in - current out:

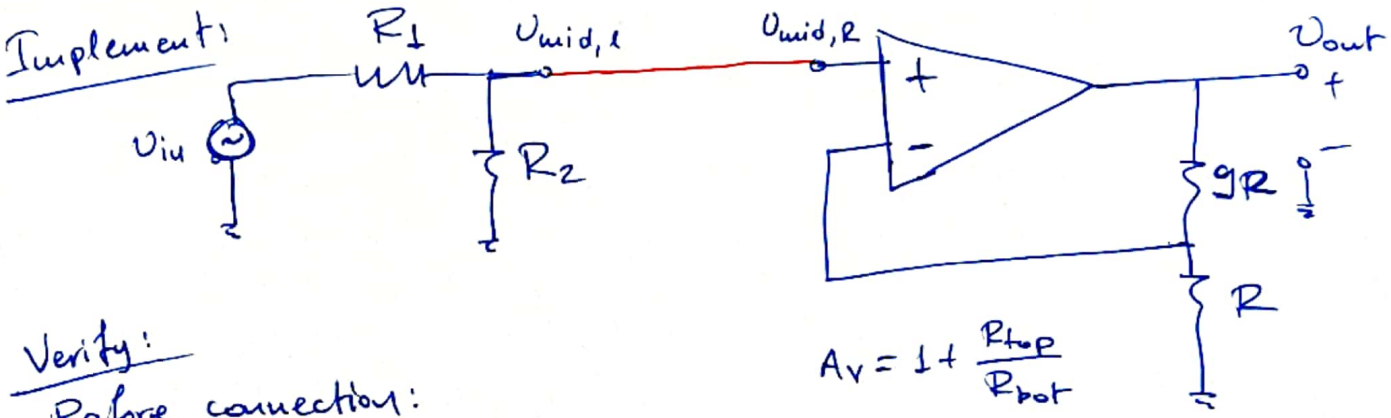
Ideally:

Example #1 : Want this:



$\hookrightarrow V_{out} = 10 \cdot V_{mid}$

Implement:



Verify:

Before connection:

$$V_{mid_1} = \frac{R_2}{R_1+R_2} \cdot V_{in}$$

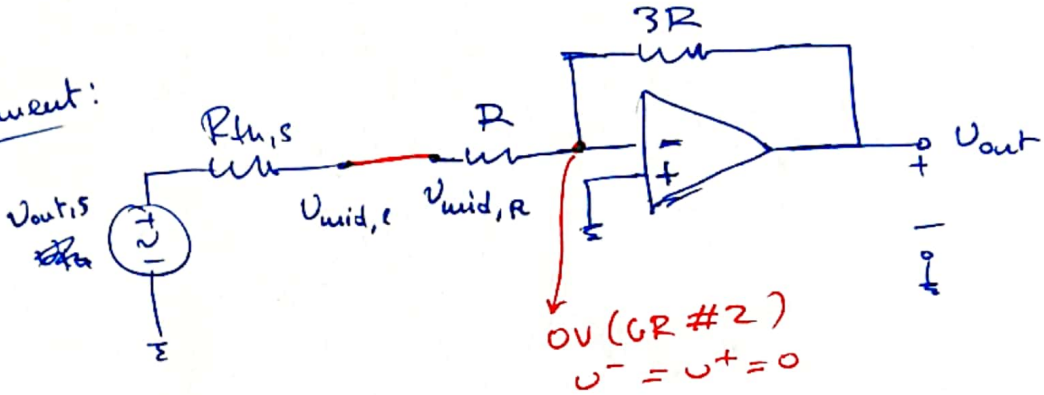
After connection:

$$V_{mid_1} = V_{mid,R} = \frac{R_2}{R_1+R_2} \cdot V_{in} \quad \ddot{\smile}$$

$$\Rightarrow V_{out} = \frac{R_2}{R_1+R_2} \cdot \underbrace{\left(1 + \frac{R_{top}}{R_{bot}}\right)}_{10} \cdot V_{in} \checkmark$$

Example #2: Want this:

Implement:



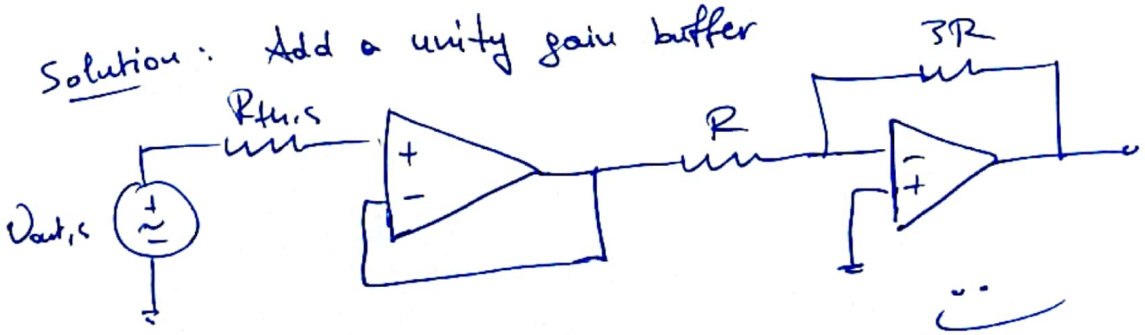
Verify: Before connection:

$v_{mid,L} = v_{out,s}$

After connection:

$v_{mid,L} = v_{mid,R} = \frac{R}{R + R_{th,s}} \cdot v_{out,s} \neq v_{out,s}$ ∴

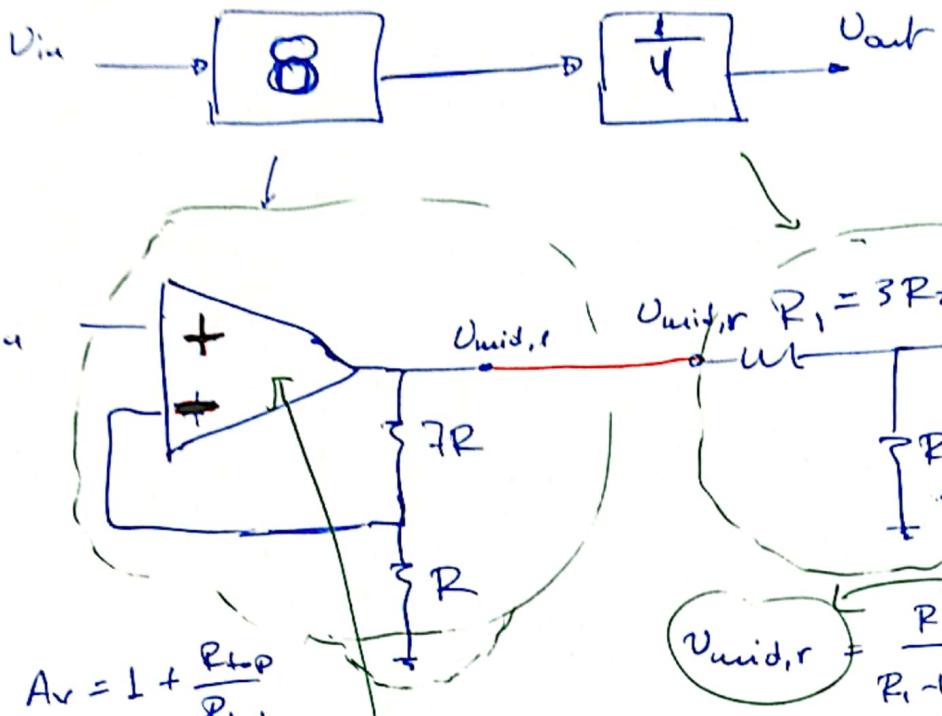
Solution: Add a unity gain buffer

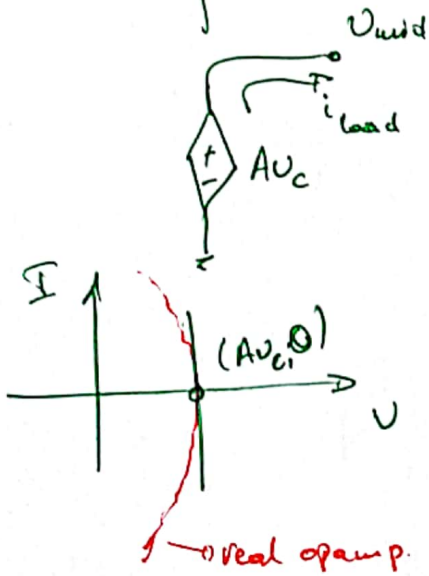


∴

(p5)

Example #3





☺

Fine because

$v_{mid,l}$ is set by AV_c (volt. source)

After comm.:

$v_{mid,l} = v_{mid} = v_{in} \cdot 8$ ✓

$v_{out} = 8 \cdot \frac{1}{4} \cdot v_{in}$ ✓

Design Procedure

Step 1: (specification) Concretely (re)-state your goal for the design (most often from a word spec)

Step 2: (Strategy) Describe (often as a block diagram) the strategy to achieve the goal.

- ↳ review what you can measure vs what you wanted to know
- ↳ what is the relationship between the two (e.g. touch/no-touch)

touch/no-touch → [change in capacitance] → [change in voltage] → binary output voltage.

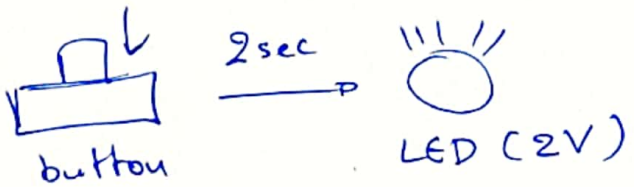
Step 3: (Implementation) Implement the components within the strategy

- ↳ Remind yourselves of you know that can provide the desired block diagram function.
- ↳ Think about how do extend/modify the blocks you know (attempt #1000)

Step 4: (Verification/analysis) Does the implementation in step 3 do what is specified in step 1?

- ↳ check for block-to-block connections

Example Design #1 Countdown timer



Step 1: (Specification) Build a circuit that after a button is pushed measure 2s and then applies 2V across an LED. (I assume you can only push the button once).

Step 2: (Strategy) Push the button → Turn-on Timer → Timer → ≥ → apply 2V to LED

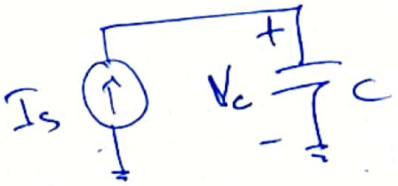
"time since button pushed"

2sec

Step 3: (Implementation)

Turn-on ckt: (switch)

Timer:



$$I_c = C \cdot \frac{dV_c}{dt}$$

$$V_c(t) = \frac{I_c}{C} \cdot t + V_c(0)$$

V_{time}

≥: