P1

Module 2, Lecture 11

EECS 16A
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Last Time:
* Safely Cascading Ckt Blocks
* Design Procedure
* Design Examples

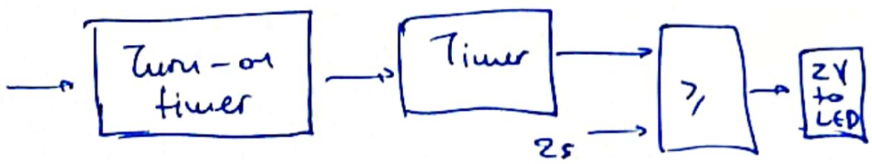
Today:
* Design Examples (Cont.)

→ Note 20

Countdown Timer Circuit (Cont.)

Step 1: (Specification) Build a circuit that after a button is pushed measures 2s and then applies 2V to an LED

Step 2: (Strategy) Push the button →

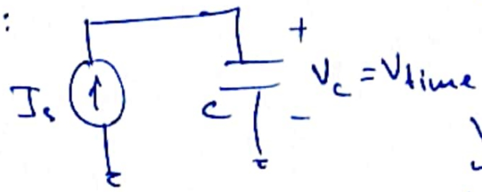


Step 3: (Implementation)

Turn-on ckt:

(switch)

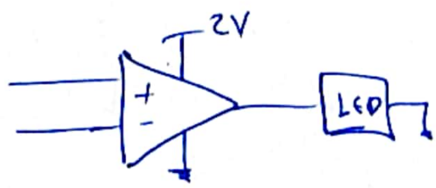
Timer:



$$I_c = C \cdot \frac{dV_c}{dt}$$

$$\underbrace{V_c(t)}_{V_{time}} = \frac{I_c}{C} \cdot t + V_c(0)$$

≥



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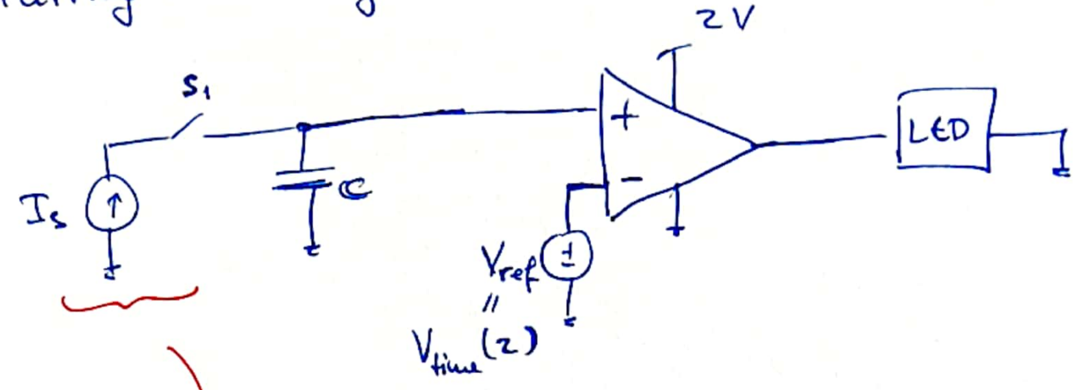
Putting it all together:

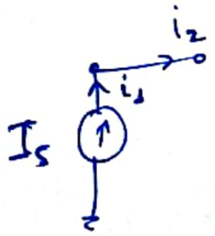


Step 4: (Verify)

$$V_c(t) = V_{time} = \frac{I_s}{C} \cdot t + V_c(0)$$

Prob. #1 — ? unknown

Before button pushed:



$i_1 = I_s$ (element (current source) I-V relationship)

$i_2 = 0$ (element (open-ckt) —||—)

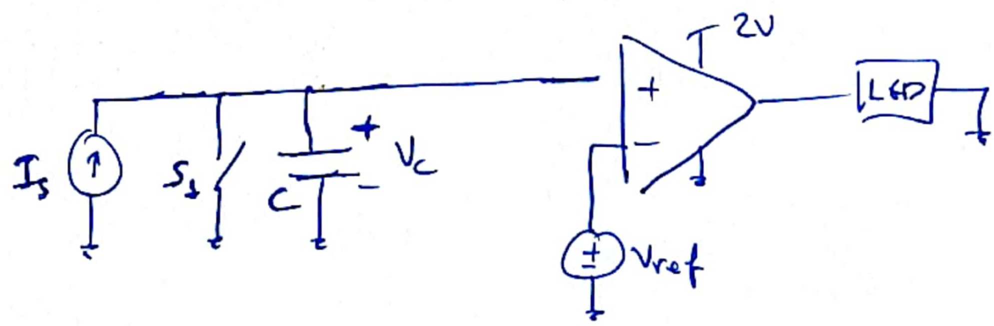
KCL: $i_1 = i_2$

↳ $I_s = 0$ contradiction/inconsistency. Prob. #2

Solutions: a) Shut-off the I_s when S_1 is OFF (impose a safe voltage limit across I_s)

b) Reconfigure the switch

Revisit Step 3 (Implem.):



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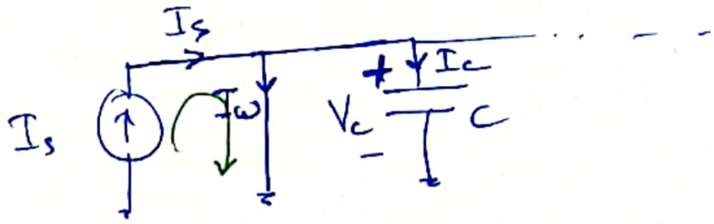
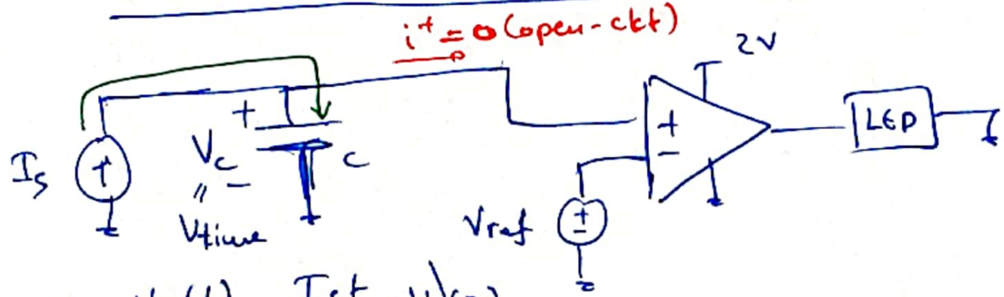
Step 4
(Verification)

Before button pushed:



$I_w = I_s$ (path of least resistance)

After button pushed: (assuming at $t=0$)



$$V_c(t) = V_{time}(t) = \frac{I_s t}{C} + V_c(0) \quad V_c(0) \to 0$$

:)

$$V_{ref} = V_c(2) = \frac{I_s}{C} \cdot 2 \quad ✓$$

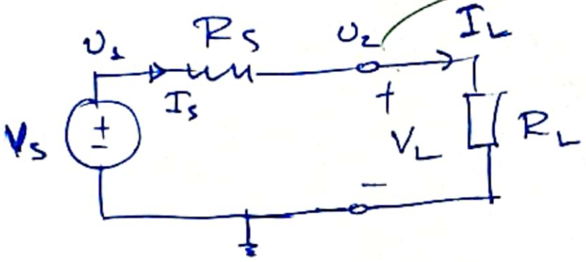
(p4) Example Design #2 : Current Source.

Step 1: (Specification) Build a circuit that can create a constant current through its output terminals regardless of the voltage across them.

To do so you can use op amps, voltage sources and resistors.

Step 2: (Strategy) Ohm's law: $V = I \cdot R \Rightarrow I = \frac{V}{R}$ → make constant

Step 3: (Implementation)

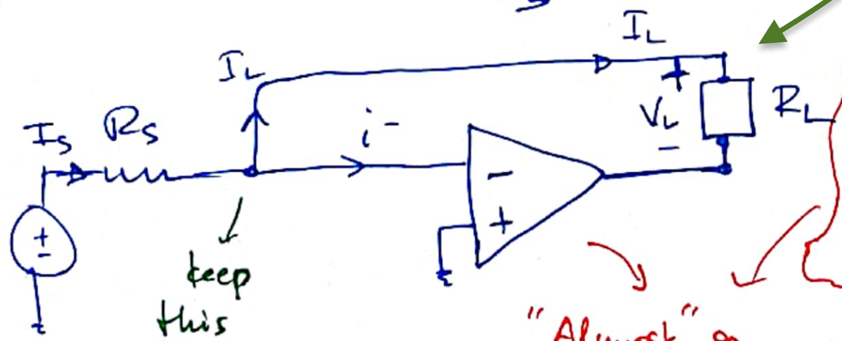


What if I could fix this voltage at 0V?

Step 4: (Verify) Ohm's law: $I_S = \frac{V_{R_S}}{R_S} = \frac{v_1 - v_2}{R_S} = \frac{V_S - V_L}{R_S}$

KCL: $I_S = I_L = \frac{V_S - V_L}{R_S} = f(V_L)$:-((since I wanted I_L indep. of V_L)

Revisit step 3: (Implem.)



"Almost" a current source

Caveats:
1) Op-Amp needs to be in NFB.
2) $v^- = 0$ may have implications for the rest of the ckt

Step 4: (Verify) $I_S = \frac{V_S}{R_S}$ (Ohm's law)

KCL at v^-: $I_S = I_L + i^-$ → 0 (GR #1)

$\Rightarrow I_L = \frac{V_S}{R_S} \neq f(V_L)$:-)

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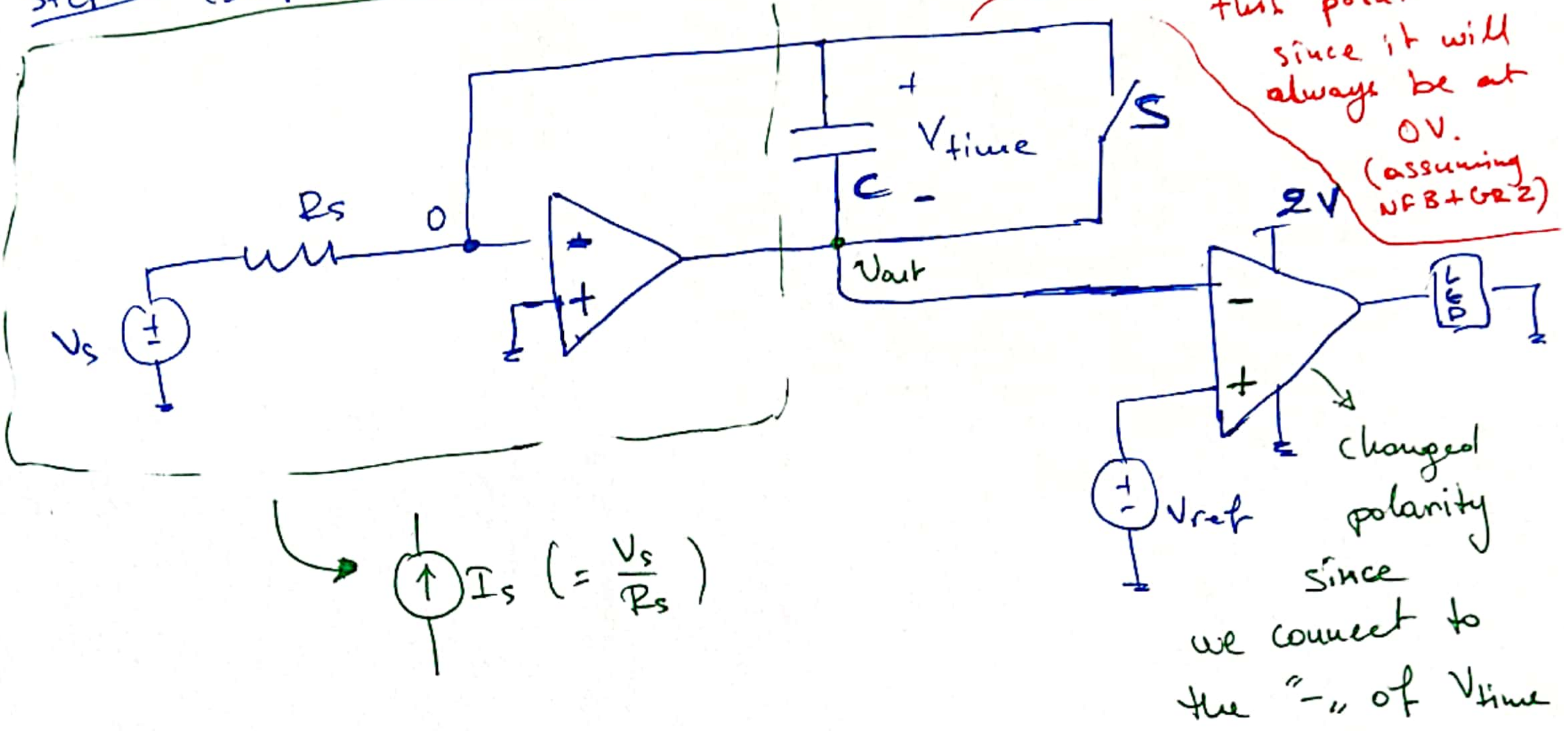
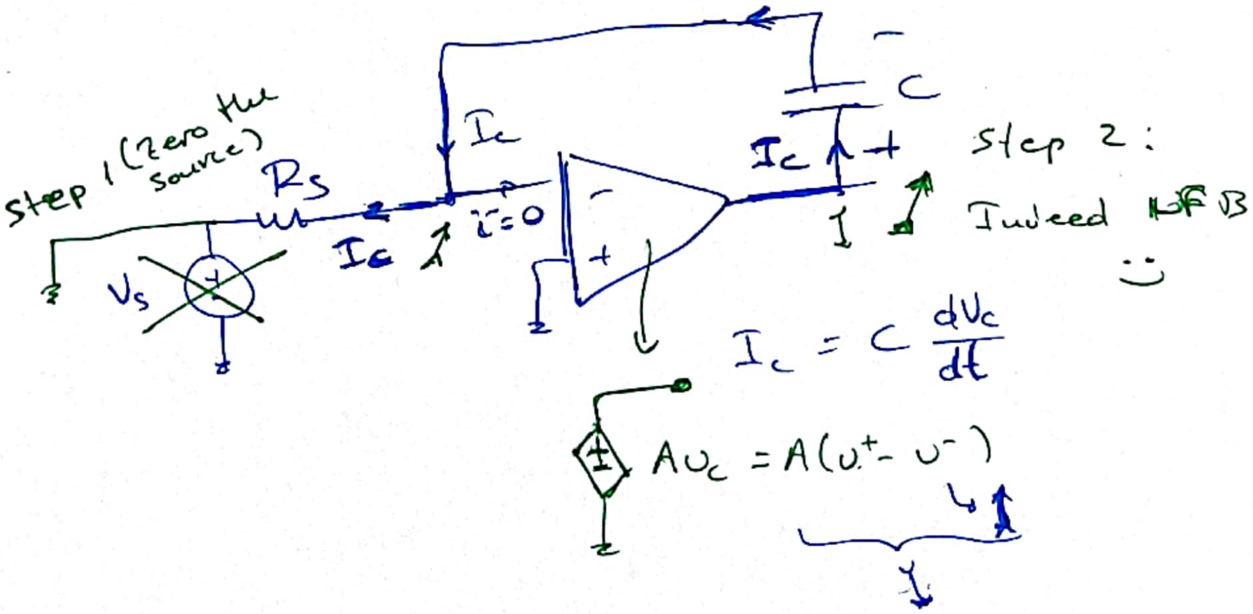
Let's tie it back to our timer circuit:

Step 3: (Implem.)



Step 4:
(verify) Check for NFB:



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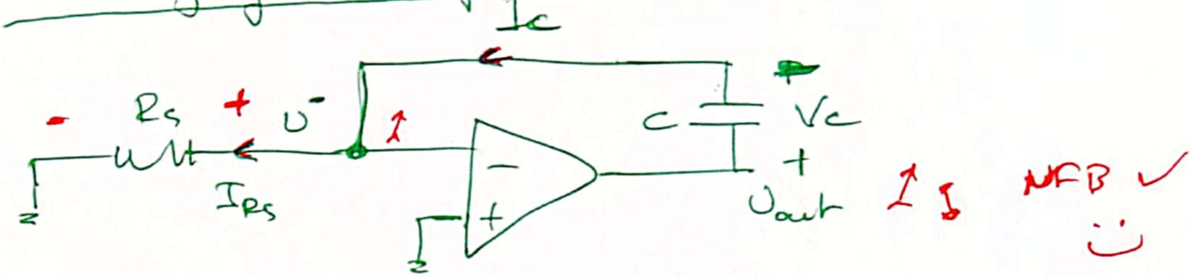
Thoroughly checking for NFB:



Steady state: i.e. all voltages are constant.

$$I_{R_s} = \frac{U^- - 0}{R_s} = \text{const.} \quad (1)$$

$$I_c = I_{R_s} \quad \begin{pmatrix} GR\#1+ \\ KCL \end{pmatrix} \quad (2)$$

$$I_c = C \cdot \frac{dV_c}{dt} \rightarrow 0 = 0 \quad (3)$$

$$(2) \overset{(3)}{\Rightarrow} I_{R_s} = 0 \overset{(1)}{\Rightarrow} U^- = 0$$

→ At steady state $U^- = 0$ w/o assuming NFB!

$I_c = I_{R_s} \Rightarrow U^- = I_{R_s} \cdot R_s > 0$

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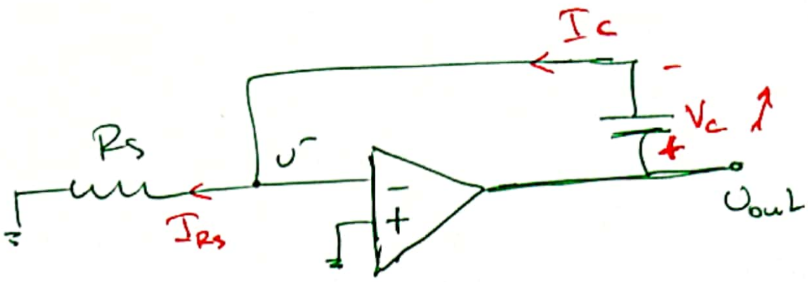


Since $v^- = 0$ at steady state let's "yank" the output ↑

$$I_c = C \cdot \frac{dV_c}{dt}$$

(Since v_{out} ↑ I_c have to obey passive sign convention and follow the ckt diagram direction).

KCL at v^-:

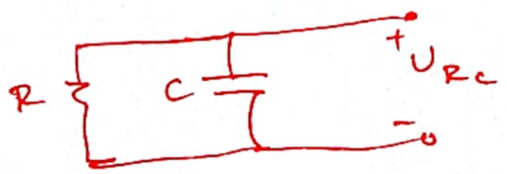
GR #1

$I_c = I_{Rs}$ (no current into the opamp)

↳ $v^- - 0 = I_{Rs} R_s \Rightarrow v^- > 0 \Rightarrow v^- \uparrow \Rightarrow v_{out} \downarrow$

$\Rightarrow$ NFB

Aside:



At steady state:

$v_{RC} = 0$

more in 16B!