

Read the following instructions before the exam.

Format & How to Submit Answers

There are 12 problems (4 introductory questions, and 8 exam questions, comprising 42 subparts total) of varying numbers of points. The problems are of varying difficulty, so pace yourself accordingly and avoid spending too much time on any one question until you have gotten all of the other points you can. Don't get bogged down in calculations; if you are having trouble with one problem, there may be easier points available later in the exam!

All answers will be submitted to the Gradescope "Midterm 2" Assignment (<https://www.gradescope.com/courses/137582/assignments/576104>). All questions, except introductory questions, are multiple choice and are **worth 3 or 4 points each**. **There are 150 points possible on the exam, but your final score will be taken out of 140 points.** This means that a score of 100/150, normally 67%, will be bumped up to 100/140, or 71%. You cannot score more than 100% on this exam.

Partial credit may be given for certain incorrect answer choices for some problems. There is no penalty for incorrect answers.

Post any content or clarifying questions privately on Piazza. There will be no exam clarifications; if we find a bug on the exam, that sub-question will be omitted from grading.

Timing & Penalties

You have 120 minutes for the exam, with a 5 minute grace period. After the 5 minute grace period ends, exam scores will be penalized exponentially as follows: an exam that is submitted N minutes after the end of the grace period will lose 2^N points. **The exam will become available at your personalized link at 7:10 pm PT; the grace period will expire at 9:15 pm PT.** If your submission is timestamped at 9:16 pm PT, you will lose 2 points; if it is timestamped at 9:18 pm PT, you will lose 8 points.

We will count the latest time at which you submit any question as your exam timestamp. Do NOT edit or resubmit your answers after the deadline. We recommend having all of your answers input and submitted by 9:10 pm; it is your responsibility to submit the exam on time.

If you cannot access your exam at your link by 7:15 pm, please email eeecs16a@berkeley.edu. If you are having technical difficulties submitting your exam, you can email your answers (either typed or scanned) to eeecs16a@berkeley.edu.

Academic Honesty

This is an open-note, open-book, open-internet, and **closed-neighbor** exam. You may use any calculator or calculation software that you wish, including Wolfram-Alpha and Mathematica. **No collaboration is allowed, and do not attempt to cheat in any way. Cheating will not be tolerated.**

We have zero tolerance against violation of the Berkeley Honor Code. Given supporting evidence of cheating, we reserve the right to automatically fail all students involved and report the instance to the student conduct committee. We reserve the right to **audit students with oral exams** after the midterm to ensure academic honesty. Feel free to report suspicious activity through this form. (<https://forms.gle/ZzXLksZEmx9bn1mj7>).

Our advice to you: if you can't solve a particular problem, move on to another, or state and solve a simpler one that captures at least some of its essence. You will perhaps find yourself on a path to the solution.

Good luck!

EECS 16A Designing Information Devices and Systems I
Summer 2020 Midterm 2

1. Pledge of Academic Integrity (2 points)

By my honor, I affirm that:

- (1) this document, which I will produce for the evaluation of my performance, will reflect my original, bona fide work;
- (2) as a member of the UC Berkeley community, I have acted and will act with honesty, integrity, and respect for others;
- (3) I have not violated—nor aided or abetted anyone else to violate—nor will I—the instructions for this exam given by the course staff, including, but not limited to, those on the cover page of this document; and
- (4) I have not committed, nor will I commit, any act that violates—nor aided or abetted anyone else to violate—the UC Berkeley Code of Student Conduct.

Write your name and the current date as an acknowledgement of the above. (See Gradescope)

2. Administrivia (2 points)

I know that I will lose 2^n points for every n minutes I submit after the exam submission grace period is over.

For example, if the exam becomes available at my personalized link at 7:10 p.m. PT; the grace period will expire at 9:15 p.m. PT. If my submission is timestamped at 9:16 p.m. PT, I will lose 2 points; if it is timestamped at 9:18 p.m. PT, I will lose 8 points.

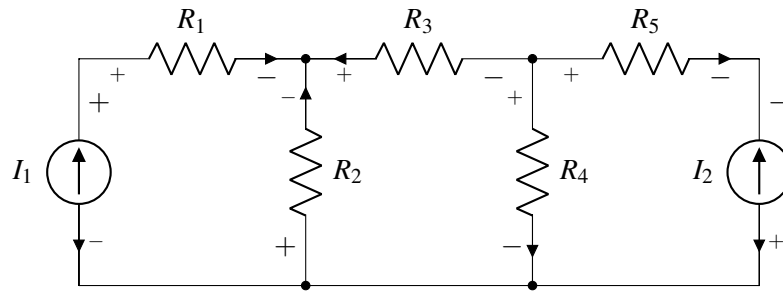
- Yes

3. What do you enjoy most about EECS16A? (2 points)

4. Tell us about something that makes you happy. (2 points)

5. Circuit Analysis (12 points)

(a) (4 points) Which components have been labeled according to passive sign convention? Select all that apply.

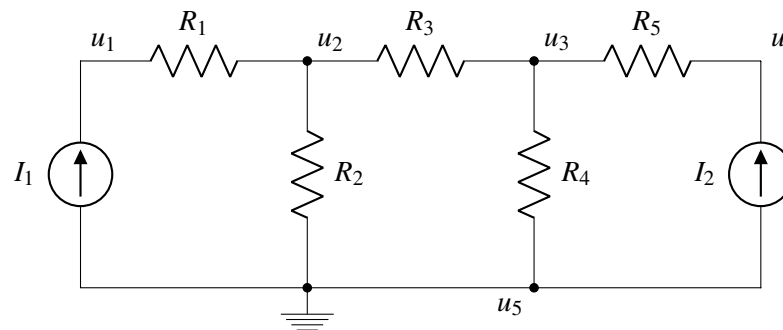


- | | |
|-----------|-----------|
| (1) I_1 | (5) R_4 |
| (2) R_2 | (6) R_5 |
| (3) R_1 | (7) R_3 |
| (4) I_2 | |

Solution: The only elements that have the current flowing into positive and coming out the negative voltage labelings are R_1, R_2, R_4, R_5, I_1 .

Note that I_2 does not follow passive sign convention and I_1 does because it is the labeled current on the branch relative to the labeled voltage polarity matters, not the current within the circle of the current source symbol.

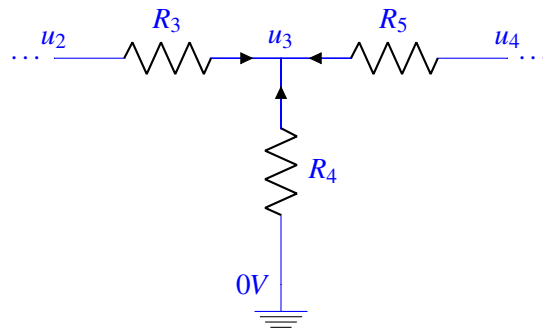
(b) (4 points) Find the correct KCL expression at the node with node voltage u_3 .



Solution:

$$\frac{u_2 - u_3}{R_3} + \frac{0 - u_3}{R_4} + \frac{u_4 - u_3}{R_5} = 0$$

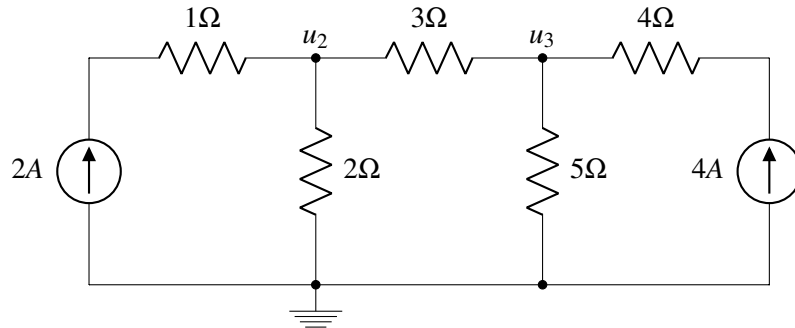
At node with node voltage u_3 , there are three resistors connected to the node, so there will be three currents entering or exiting the node. Assume the following current directions in the figure below.



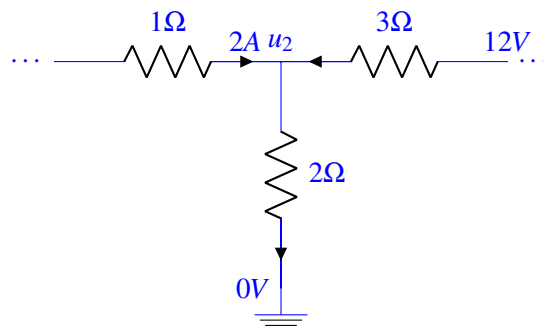
This leads to the following KCL expression: $\frac{u_2 - u_3}{R_3} + \frac{0 - u_3}{R_4} + \frac{u_4 - u_3}{R_5} = 0$.

If the above current directions were not assumed, the same KCL equation can still be acquired. If a current was assumed leaving, it would appear on the other side of the equation as a negated version of one of the terms in the answer.

(c) (4 points) Given the node voltage $u_3 = 12V$, find u_2 .



Solution: Consider the following current direction labelings at the u_2 node. Note that the current coming into the u_2 node from the left through the 1Ω resistor is $2A$ as the current source is in series with the 1Ω resistor.



From KCL at the u_2 node:

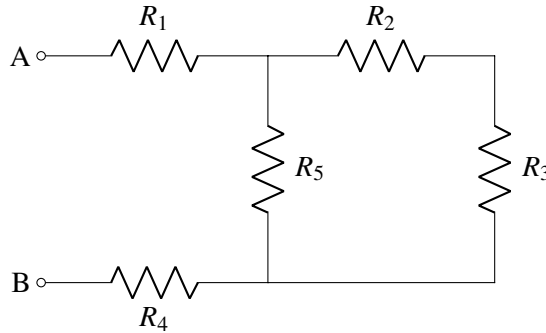
$$\begin{aligned}2A + \frac{12V - u_2}{3\Omega} &= \frac{u_2 - 0V}{2\Omega} \\6\Omega \left(2A + \frac{12V - u_2}{3\Omega} \right) &= 6\Omega \left(\frac{u_2 - 0V}{2\Omega} \right) \\12V + 24V - 2u_2 &= 3u_2 \\36V &= 5u_2 \\u_2 &= \frac{36}{5}V\end{aligned}$$

6. Equivalence in Resistive and Capacitive Networks (15 points)

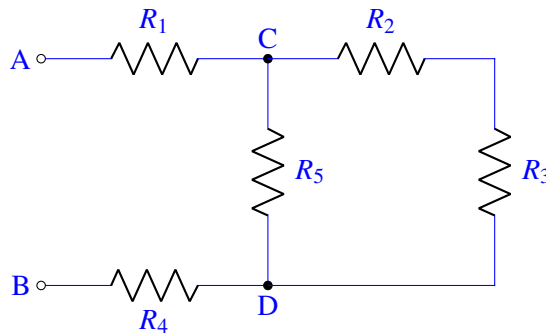
For all of the following networks find an expression or a numerical value for the equivalent resistance or capacitance between terminals A and B.

Hint: You can use the equivalence formulas for series and parallel combinations of resistors and capacitors for all of the subparts in this question.

(a) (3 points)

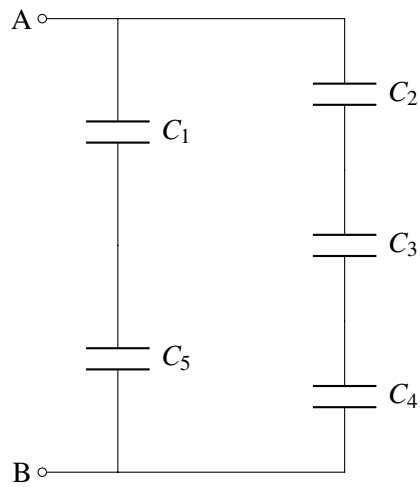


Solution:



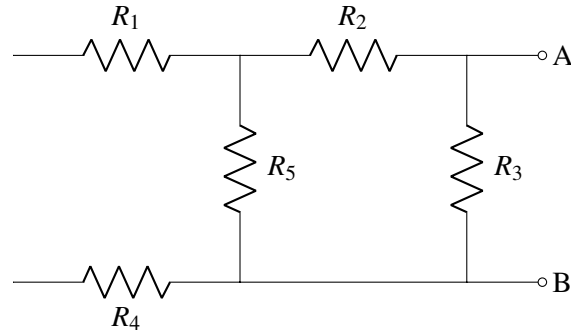
The easiest way to simplify a network if unsure, is to label more nodes and try to make smaller simplifications steps. For example, after introducing terminals C and D, we can see that we can represent the equivalent resistance in between those terminals as R_5 in parallel with the series combination of R_2 and R_3 , so $R_{CD} = R_5 || (R_2 + R_3)$. Finally, we can see that R_{CD} is in series with both R_1 and R_4 , as we look right from terminals A, B. This gives us the final result: $R_{AB} = R_1 + R_5 || (R_2 + R_3) + R_4$.

(b) (3 points)



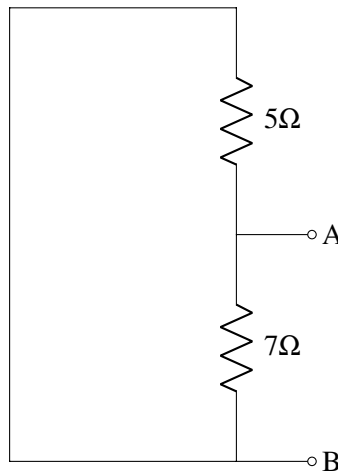
Solution: Here we have two branches connected in parallel, one including capacitors C_1 , C_5 (which are connected in series) and one including capacitors C_2 , C_3 , and C_4 (which are also connected in series). Hence, the correct answer is: $C_{AB} = (C_1 || C_5) + (C_2 || C_3 || C_4)$.

(c) (3 points)



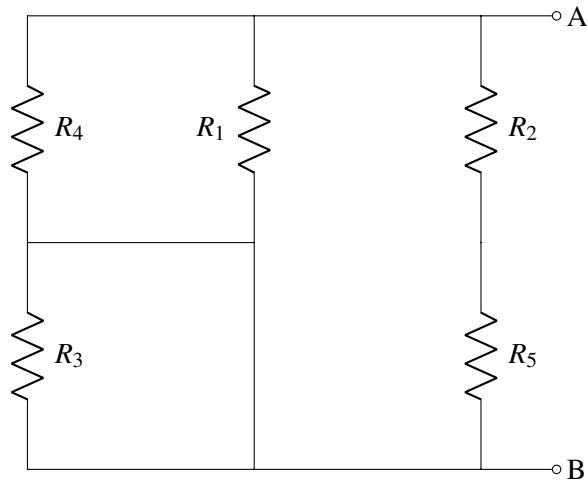
Solution: In this question it is crucial to realize, resistors R_1 and R_4 are connected to an open-circuit so they don't contribute to the overall resistance looking left from terminals A, B. After we delete them from our circuit diagram, we can get the answer as $R_{AB} = R_3 || (R_2 + R_5)$.

(d) (3 points)



Solution: Here we need to notice that terminal B is connected not only to the bottom of the 7Ω resistor, but also to the top of the 5Ω resistor. Thus, the two resistors have both terminals common, are connected in parallel and the equivalent resistance can be computed as: $R_{AB} = \frac{7\Omega \cdot 5\Omega}{7\Omega + 5\Omega} = 2.917\Omega$.

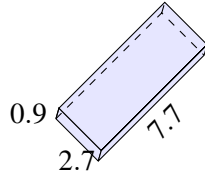
(e) (3 points)



Solution: Notice that here resistor R_3 is shorted (in other words connected in parallel with a wire). This means that it effectively can be removed from the circuit diagram, which leaves us with R_4 in parallel with R_1 and in parallel with the series combination of R_2 and R_5 , hence $R_{AB} = R_4 || R_1 || (R_2 + R_5)$.

7. Resist the Power! (23 Points)

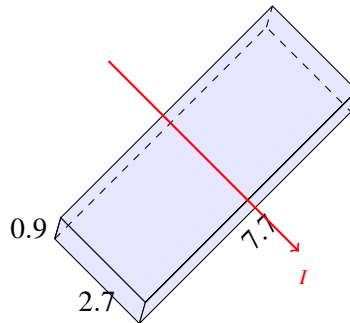
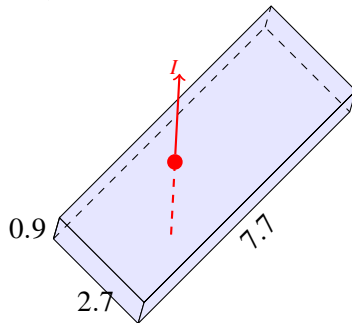
- (a) (4 points) You are given a resistive slab with resistivity $5.7\Omega \cdot \text{cm}$ and dimensions 0.9cm , 2.7cm , and 7.7cm as denoted on the figure below. The dimensions and the resistivity of the slab remain the same throughout the rest of the problem.



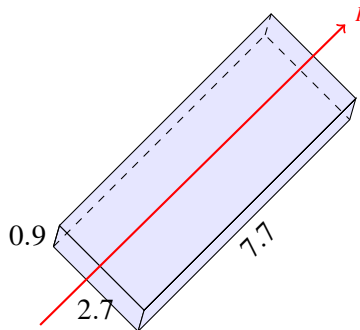
Suppose we connect opposite faces of the slab to a voltage source so that current can flow through it. Notice that there are 3 possible configurations we can have for this slab, leading to 3 possible directions in which the current can flow (drawn in the answer choices below). Which direction will lead to the **highest** current flow I assuming we use the same valued voltage source all three times?

Assume the resistivity is the same throughout the slab and does not vary with respect to the direction of current flow.

- (A) Parallel to 0.9 (current goes through 2.7, 7.7 face):
 (C) Parallel to 2.7 (current goes through 0.9, 7.7 face):



- (B) Parallel to 7.7 (current goes through 0.9, 2.7 face):
 (D) Choices (A) and (C) are tied for the maximum current flow.

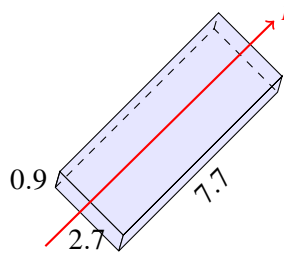


- (E) The direction doesn't matter; the resistor is physically the same, so the current will be the same.

Solution: For a given supply voltage from a voltage source, the most current will flow when the resistance of the slab is smallest. We apply the geometrical resistance formula, $R = \frac{\rho L}{A}$. To maximize

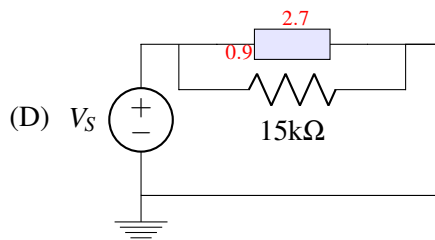
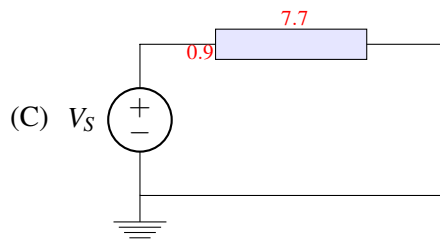
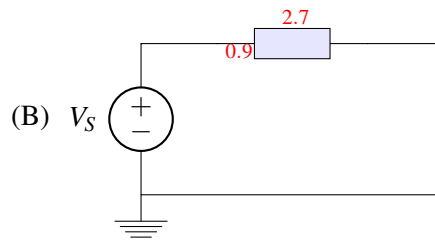
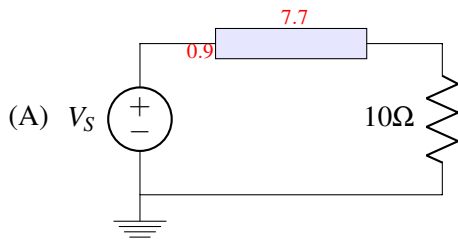
current, we need to minimize resistance, which requires minimizing L and maximizing A . Two of the dimensions will comprise the area, and the third will form the length. Noticing that $0.9\text{cm} < 2.7\text{cm} < 7.7\text{cm}$, it follows that we want to feed current into the $2.7\text{cm} \times 7.7\text{cm}$ face and use 0.9cm as the length. Therefore, we select choice (A).

- (b) (3 points) We connect the voltage source so that current flows parallel to 7.7 (through the 0.9×2.7 face), as shown below. What is the resistance of the slab, R_{slab} ?



Solution: This requires a substitution into the resistance formula: $R = \frac{\rho L}{A}$. Based on the fact that we are told to use choice (B) from (a) selected above, we find that $R_{\text{slab}} = 5.7 \left(\frac{7.7}{0.9 \cdot 2.7} \right) \Omega$.

- (c) (4 points) You are experimenting with various circuit configurations involving the slab and a voltage source. 2 dimensions are labeled (in red), and the 3rd is the one going "into" the page (not to scale). Which of the following configurations leads to the *minimum* power dissipation by the slab?



- (E) More than one of the labeled circuits has the same power dissipated across the slab.

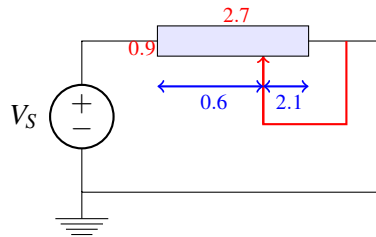
Solution: The formula for power for a resistive element is $P = IV = \frac{V^2}{R}$. To minimize power, we want to maximize the resistance and minimize the voltage drop across the slab. For resistance, given that one of the cross-sectional area terms is 0.9cm in all given circuits, if we want greater resistance, we want current to flow in the direction of 7.7cm, such that we see 7.7cm as the second-labeled dimension. Next, for voltage drop; when the slab is the only element in the circuit apart from the voltage source as shown in (C), it necessarily has a V_S volt drop across it. Adding a resistor in series decreases the voltage dropped across the slab, so power dissipation in the slab is the least in option (A).

- (d) (4 points) Suppose you selected configuration (A) from above, which may or may not be correct. What is the power dissipated by the slab in that configuration?

Solution: Knowing that $P = \frac{V^2}{R}$, we can plug in directly, using $a \cdot b$ as the area and c as the length. We account for the voltage divider on the series resistance; the voltage drop across the slab is $V_S \cdot \frac{5.7 \cdot 7.7}{0.9 \cdot 2.7 + 10}$.

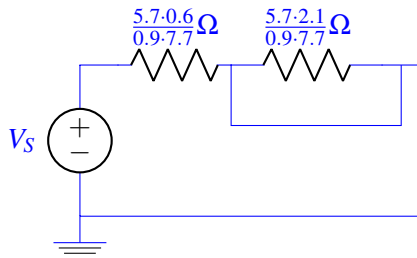
The resulting answer is $P = \frac{V^2}{R} = \frac{\left(V_S \cdot \frac{5.7 \cdot 7.7}{0.9 \cdot 2.7 + 10} \right)^2}{\frac{5.7 \cdot 7.7}{0.9 \cdot 2.7} \Omega}$.

- (e) (4 points) You realize that you can turn the slab into a variable resistor! You attach an ideal metal connector (shown in red) between one end of the resistive slab and some point in the middle of the slab, as shown below.



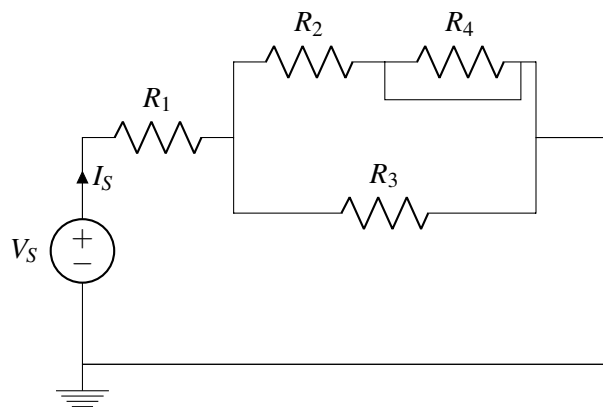
Draw the equivalent circuit diagram for this physical configuration.

Solution: Recognizing that the red metal connection acts as a short, dividing the slab into "effective" and "ineffective" components, we can model the connection as an ideal short, and the original resistor is cut into 2 portions.



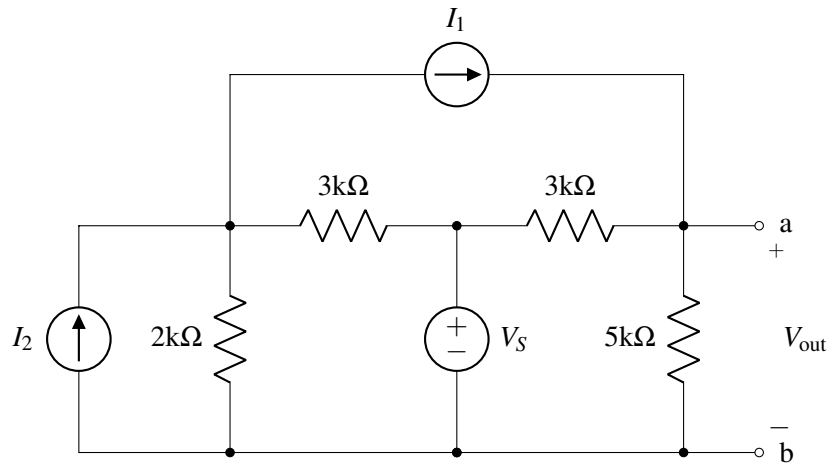
- (f) (4 points) You construct a new circuit using several resistive slabs, a variable resistor and a voltage source, for which the equivalent circuit diagram is shown below. Which resistor has **no** current passing through it, regardless of its value? Which resistor has the **most** current passing through it, regardless of its value?

Note: Assume $R_1 - R_4$ are finite positive value resistors (non-zero and non-infinite).



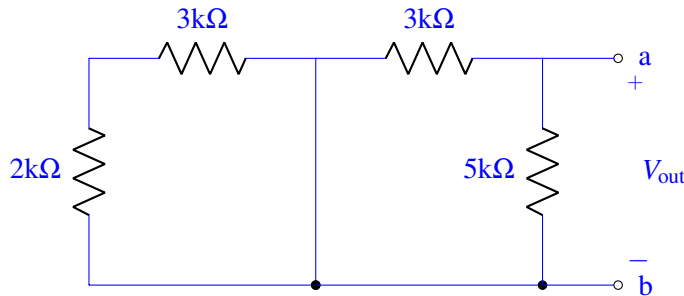
Solution: Note that R_4 is shorted by the ideal metal connector, whereas none of the other resistors are. Also, R_1 has the most current through it. We find that: no current: R_4 ; most current: R_1 .

8. Superimposing Thevenin (16 points)



- (a) (4 points) Calculate the Thevenin equivalent resistance between terminals a, b. Round to three decimal places if necessary.

Solution: To find R_{th} , we first null all of the independent sources in the circuit. Replacing the voltage source with a short circuit and the two current sources with open circuits leaves us with the circuit below.

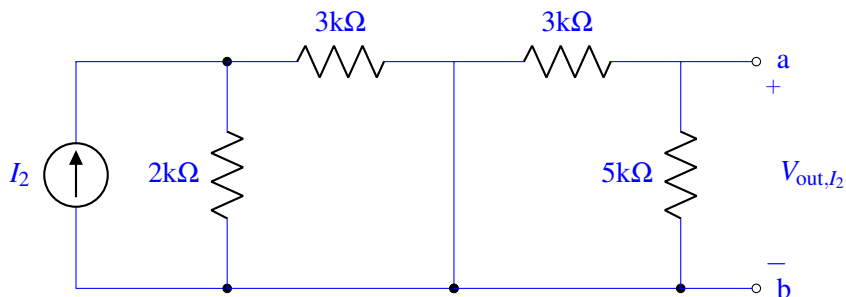


To find the equivalent resistance from the perspective of terminals a and b, we apply a "test current" to terminals a and b and deduce that any current flowing through the 5 kΩ resistor would flow through the top right 3 kΩ resistor, and then back down to node b through the short circuit created by nulling the voltage source. The top left 3 kΩ resistor and the 2 kΩ resistor are irrelevant, as I_{test} will never flow through that branch of the circuit; our R_{th} is thus $5k\Omega || 3k\Omega = \frac{5 \cdot 3}{5+3} = 1.875k\Omega$.

- (b) (4 points) Calculate the output voltage V_{out} when all sources except I_2 are nulled.

Solution:

To null all sources except I_2 , we replace V_S with a short circuit and I_1 with an open circuit.

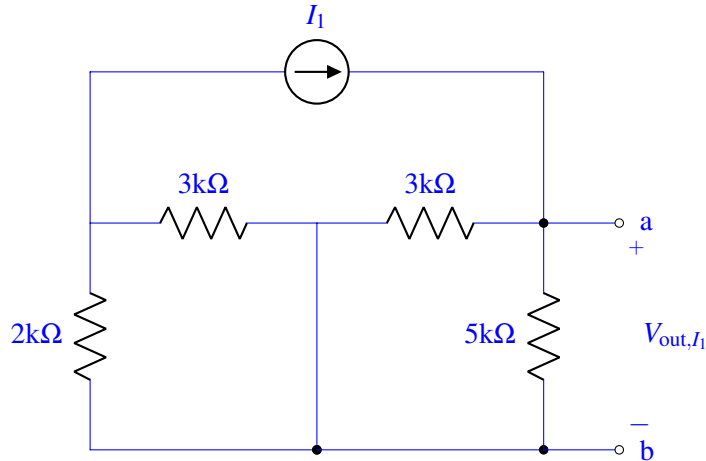


Any current I_1 will flow through the short circuit where V_S used to be; there will thus be 0V across the $5k\Omega$ resistor. $V_{out} = 0V$.

- (c) (4 points) Calculate the output voltage V_{out} when all sources except I_1 are nulled.

Solution:

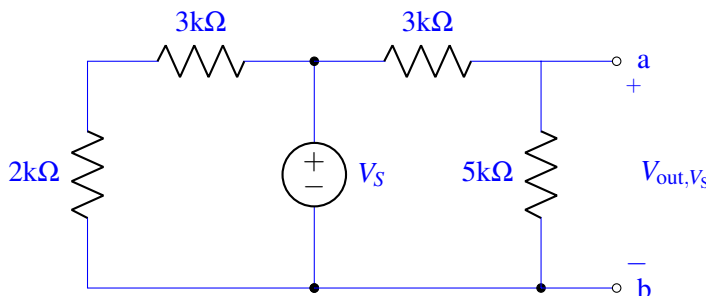
To null all sources except I_1 , we replace V_S with a short circuit and I_2 with an open circuit.



The voltage drop between terminals a and b can be found by computing a current divider between a $3k\Omega$ resistor and a $5k\Omega$ resistor. The current through the $5k\Omega$ resistor is $\frac{3}{8}I_1$. Thus, $V_{out} = \frac{3}{8}I_1 \cdot 5k\Omega = \frac{15}{8}k\Omega \cdot I_1$.

- (d) (4 points) Let αI_2 be the correct answer to part (b), and let βI_1 be the correct answer to part (c). Calculate the Thevenin equivalent voltage between the terminals a, b.

Solution: Using superposition to find the total voltage V_{out} , we've already calculated the voltage V_{out,I_1} (with all sources except I_1 nulled), and V_{out,I_2} (with all sources except I_2 nulled), in parts (b) and (c) (the results of which are taken to be αI_2 and βI_1). Because $V_{out} = V_{out,I_1} + V_{out,I_2} + V_{out,V_S}$, we need to find V_{out,V_S} .



In this circuit, the voltage drop V_{out,V_S} is computed using a voltage divider between a $5k\Omega$ and a $3k\Omega$ resistor. $V_{out,V_S} = V_S \frac{5}{5+3} = \frac{5}{8}V_S$. Thus, $V_{out} = \alpha I_2 + \beta I_1 + \frac{5}{8}V_S$.

9. Misadventures with Measurements (20 points)

You are learning about voltmeters and ammeters in EECS 16A Module 2. A voltmeter is an instrument used to measure the voltage difference between any two nodes in a circuit, while an ammeter measures the current through any circuit element. We can model the voltmeter and the ammeter as resistors: R_{VM} and R_{AM} respectively.

- (a) (4 points) Suppose we want to measure the voltage across nodes a and b (V_{ab}) in the circuit on the left in Figure 1. To accomplish this, we connect the voltmeter across nodes a and b , as shown on the right in Figure 1.

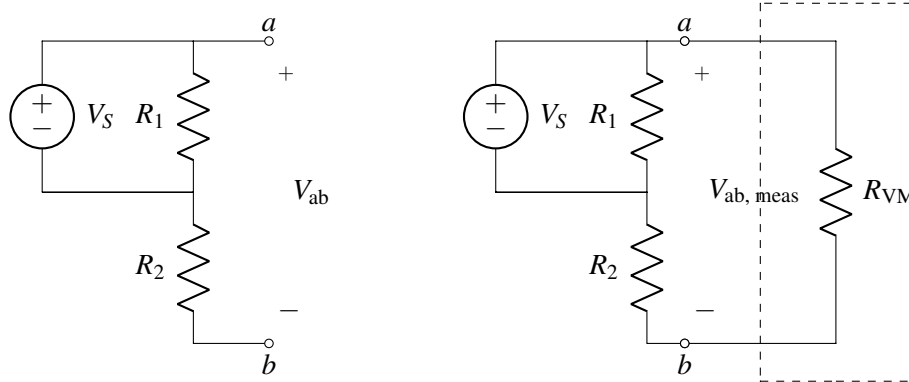


Figure 1: Left: Circuit without the voltmeter connected, Right: Voltmeter measuring $V_{ab, meas}$

Assuming that $R_{VM} \rightarrow \infty$, what is the value of voltage $V_{ab, meas}$ approximately, in terms of R_1 , R_2 , R_{VM} , and V_S ?

Solution: Using voltage divider rule:

$$V_{ab, meas} = V_S \frac{R_{VM}}{R_{VM} + R_2} \quad (1)$$

(2)

Since $R_{VM} \gg R_1, R_2$, $(R_{VM} + R_2) \approx R_{VM}$. Hence,

$$V_{ab, meas} \approx V_S \frac{R_{VM}}{R_{VM}} \quad (3)$$

$$\implies V_{ab, meas} \approx V_S \quad (4)$$

- (b) (4 points) For this part, let's assume that $V_S = 5V$, $R_{VM} = 490k\Omega$ for Figure 1. (In this case, the voltmeter is non-ideal and R_{VM} is comparable to R_1 and R_2). This non-ideality causes a discrepancy between the voltage V_{ab} before connecting the voltmeter and the measured voltage, $V_{ab, meas}$. The percentage error is given by

$$\%err = \frac{V_{ab} - V_{ab, meas}}{V_{ab}} \times 100\% \quad (5)$$

Find all the combinations of R_1 and R_2 that keep the % error below 1%.

- (1) $R_1 = 5.0k\Omega$, $R_2 = 6.1k\Omega$

- (2) $R_1 = 5.0\text{k}\Omega, R_2 = 10.1\text{k}\Omega$
 (3) $R_1 = 10.1\text{k}\Omega, R_2 = 4.9\text{k}\Omega$
 (4) $R_1 = 6.1\text{k}\Omega, R_2 = 5.0\text{k}\Omega$
 (5) $R_1 = 5.0\text{k}\Omega, R_2 = 4.9\text{k}\Omega$

Solution: From the last part we have,

$$V_{ab, \text{meas}} = V_S \frac{R_{VM}}{R_{VM} + R_2} \quad (6)$$

(7)

Substituting the value of $V_{ab, \text{meas}}$, we have

$$\%err = \frac{V_{ab} - V_{ab, \text{meas}}}{V_{ab}} \times 100\% < 1\% \quad (8)$$

$$\implies \frac{V_S - V_S \frac{R_{VM}}{R_2 + R_{VM}}}{V_S} \times 100\% < 1\% \quad (9)$$

$$\implies \frac{R_2}{R_2 + R_{VM}} < 0.01 \quad (10)$$

$$\implies R_2 < 0.01R_2 + 0.01 \times 490\text{k}\Omega \quad (11)$$

$$\implies R_2 < 4.9\text{k}\Omega/0.99 \quad (12)$$

$$\implies R_2 < 4.95\text{k}\Omega \quad (13)$$

(14)

R_1 can have any value. Thus, options (3) and (5) are correct.

- (c) (4 points) Now let us modify the previous circuit by short circuiting terminals a and b , as shown on the left of Figure 2. Suppose we want to measure the current through R_2 . To do so, we insert an ammeter in series with R_2 , as shown on the right in Figure 2.

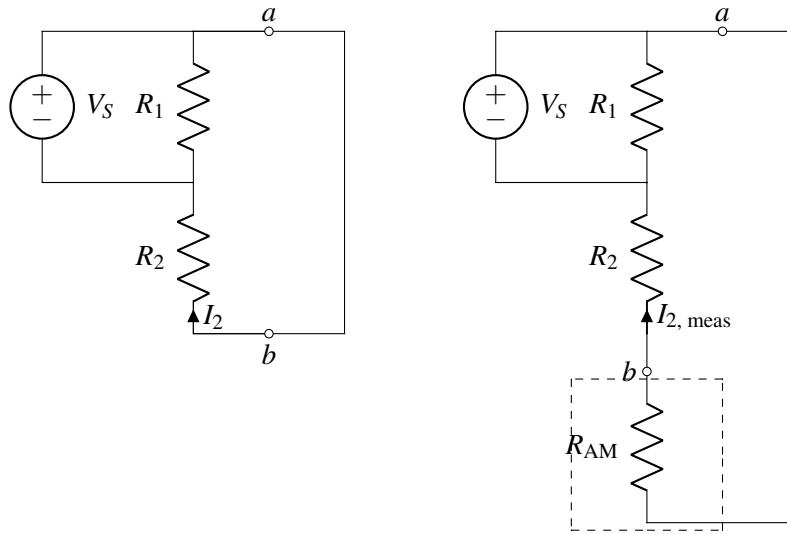


Figure 2: Left: Circuit without the ammeter connected, Right: ammeter measuring I_2

Assuming that $R_{AM} \rightarrow 0$, what is the value of the current $I_{2, \text{meas}}$ approximately, in terms of R_1 , R_2 , R_{AM} , and V_S ?

Solution: Using Ohm's law, we have:

$$I_{2, \text{meas}} = \frac{V_S}{R_2 + R_{AM}} \quad (15)$$

(16)

Since $R_{AM} \ll R_1, R_2$, $(R_2 + R_{AM}) \approx R_2$. Hence,

$$I_{2, \text{meas}} \approx \frac{V_S}{R_2} \quad (17)$$

(18)

- (d) (4 points) A photoresistor is a special kind of resistor, whose resistance decreases when we shine light on it. We introduce a photoresistor, R_{Ph} , in the circuit from the last part, arriving at the circuit in Figure 3. Depending on the light intensity, R_{Ph} varies between 100Ω and $100k\Omega$. Here we assume that $V_S = 5V$, $R_{AM} = 100\Omega$ (non-ideal ammeter).

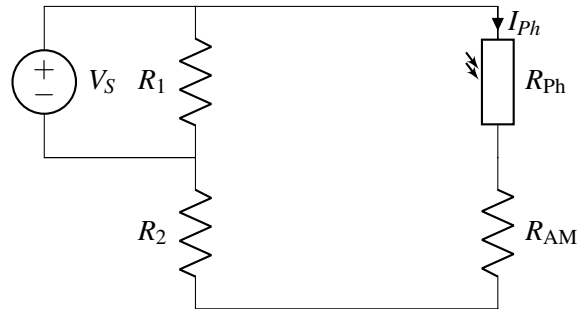


Figure 3: Circuit with ammeter measuring I_{Ph} through the photoresistor

We want the maximum current through R_{Ph} to stay below 1.0mA . Choose value(s) of R_2 to make sure that $I_{Ph} < 1.0\text{mA}$ for the full range of R_{Ph} . Choose all the options that are applicable.

- (1) $R_2 = 4750.0\Omega$
- (2) $R_2 = 4850.0\Omega$
- (3) $R_2 = 4900.0\Omega$
- (4) I_{Ph} does not depend on R_2
- (5) $R_2 = 4700.0\Omega$
- (6) None of these options are correct

Solution: Using Ohm's law, we have:

$$I_{Ph} = \frac{V_S}{R_2 + R_{AM} + R_{Ph}} < 1.0\text{mA} \quad (19)$$

$$\Rightarrow R_2 + R_{AM} + R_{Ph} > \frac{V_S}{1.0\text{mA}} \quad (20)$$

$$\Rightarrow R_2 > \frac{V_S}{1.0\text{mA}} - R_{AM} - R_{Ph} \quad (21)$$

$$\Rightarrow R_2 > \frac{5}{1.0\text{m}} - 100 - 100 \quad (22)$$

$$\Rightarrow R_2 > 4800.0k\Omega \quad (23)$$

Options (2) and (3) are correct.

- (e) (4 points) For this part, let's assume that the voltmeter and ammeter are ideal, i.e. $R_{VM} \rightarrow \infty$ and $R_{AM} = 0\Omega$.

Values of V_S , R_1 and R_2 are unknown. Let us revisit the circuits from parts (a) and (c).

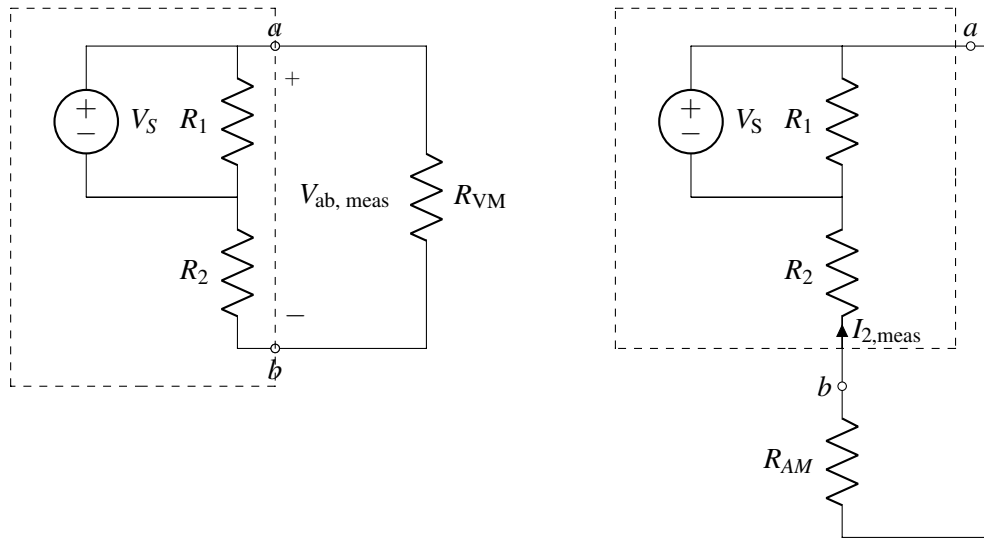


Figure 4: Left: Voltmeter measuring $V_{ab, \text{meas}}$, Right: ammeter measuring $I_{2, \text{meas}}$

We measure $V_{ab, \text{meas}} = 2\text{V}$ for the circuit on the left in Figure 4, while we measure $I_{2, \text{meas}} = 1.0\text{mA}$ for the circuit on the right. Find the Thevenin equivalent of the circuit in the box between terminals a and b , i.e. find V_{TH} and R_{TH} .

Solution: From the circuit on the left side:

$$V_{TH} = V_{ab, \text{meas}} \quad (24)$$

$$\implies V_{TH} = 2\text{V} \quad (25)$$

From the circuit on the right side, we have the short circuit current, I_{SC} :

$$I_{SC} = I_{2, \text{meas}} \quad (26)$$

$$\implies I_{SC} = 1.0\text{mA} \quad (27)$$

We can find the Thevenin resistance from:

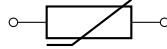
$$R_{TH} = \frac{V_{TH}}{I_{SC}} \quad (28)$$

$$\implies R_{TH} = \frac{2\text{V}}{1.0\text{mA}} \quad (29)$$

$$\implies R_{TH} = 2.0\text{k}\Omega \quad (30)$$

10. Thermostat (12 points)

Your house is too cold! You've decided to design a thermostat that will turn on the heater if the temperature is below a certain threshold, and turn off the heater once the house gets warm enough. In order to implement it, you've decided to use a new component known as a thermistor, which is represented in circuit diagrams with the following symbol:

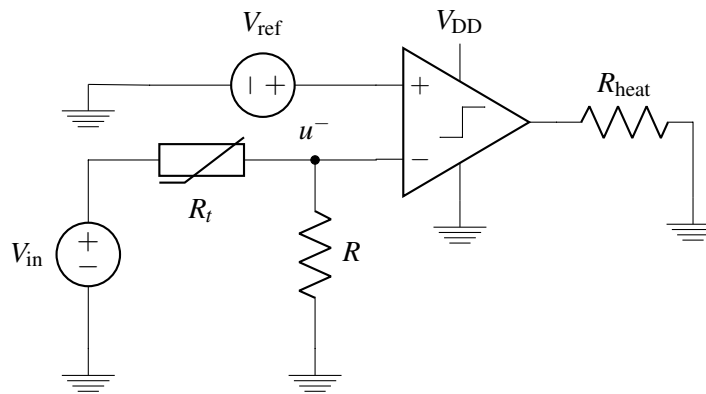


A thermistor is a variable resistor where the resistance changes with the temperature. For this problem we will be using a thermistor where the resistance increases as the temperature decreases, according to the following equation:

$$R_t = R_0 - k(T - T_0) \quad (31)$$

where T is the current temperature, R_0 is the resistance that occurs at the reference temperature T_0 , and k is a positive constant representing the sensitivity of the thermistor.

- (a) (4 points) In an old 16A textbook, you find the following circuit diagram that you think might be useful:



What is the voltage at the negative input of the comparator, u^- ? Write your answer in terms of V_{in} , R , R_0 , k , and T_0 .

Solution: Because no current flows into the terminal of an ideal comparator, we can identify the circuit at the negative terminal of the comparator as a voltage divider where $V_{out} = u^-$, and use the voltage divider equation accordingly, which gives us the following equation:

$$u^- = \frac{RV_{in}}{R_t + R}$$

To get the answer in terms of the desired variables, we can use the equation for R_t to substitute into the previous equation to get the following result:

$$u^- = \frac{RV_{in}}{R_0 - k(T - T_0) + R}$$

- (b) (4 points) The comparator should output V_{DD} when the temperature is less than T_d , the desired temperature, turning the heater on, and it should output ground otherwise, turning the heater off. Based on the part (a) diagram and equation 31, express T_d , the point at which the thermostat switches off the heat, as a function of V_{in} , V_{ref} , V_{DD} , R , R_0 , k , and T_0 .

Solution: We know that T_d is the temperature where the comparator switches on and off, which means it is the temperature where the voltage at the positive terminal is equal to the voltage at the negative terminal. Using that information, we can apply the voltage divider equation to the negative terminal to get this equation:

$$V_{ref} = \frac{RV_{in}}{R + R_t}$$

Using Equation (2), we can rewrite R_t in terms of T_d to get

$$V_{ref} = \frac{RV_{in}}{R + R_0 - k(T_d - T_0)}$$

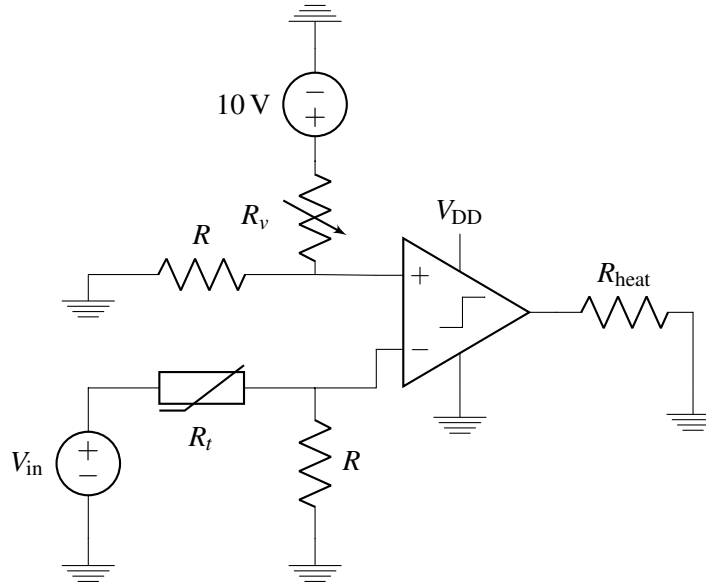
Finally, we can rearrange the equation to solve for T_d , getting a final answer of

$$T_d = T_0 + \frac{V_{ref}(R + R_0) - RV_{in}}{kV_{ref}}$$

- (c) (4 points) In order to make it possible to change the setting of the thermostat after the thermistor has been picked, you've added a variable resistor, R_v , to your circuit. It has the following symbol:



The new circuit that you have configured is shown below.



You want to make sure that your thermostat can heat your home up to 85°F , but no more than that. To that end you have picked $V_{\text{in}} = 10\text{ V}$, $R = 8\text{ k}\Omega$, $V_{\text{DD}} = 100\text{ V}$, $R_{\text{heat}} = 5\ \Omega$, and a thermistor with $R_0 = 4\text{ k}\Omega$, $T_0 = 65^\circ\text{F}$, and $k = 10\ \Omega/^\circ\text{F}$. What is the range of R_v values that achieves this design goal?

Solution: In this new circuit diagram, we have voltage dividers on the positive and negative terminals that have identical component values except for R_v and R_t . Therefore, in order to set our desired temperature, we just have to make sure that $R_v = R_t$ at that temperature.

First, you can solve for the value that R_v must be in order for the thermostat to be set to 85°F . Setting R_v equal to the equation for R_t at 85°F , we get the following equation:

$$R_v = R_0 - k(85 - T_0) = R_0 - 20k = 4\text{ k}\Omega - 0.2\text{ k}\Omega = 3.8\text{ k}\Omega$$

Therefore, $3.8\text{ k}\Omega$ is the threshold value for R_v .

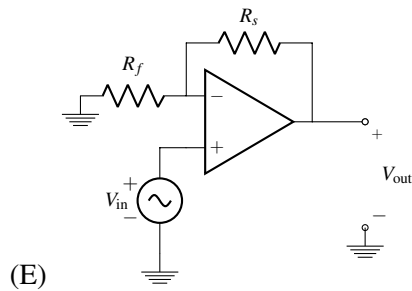
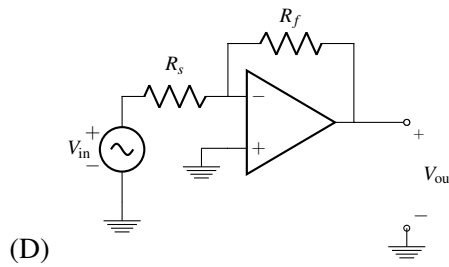
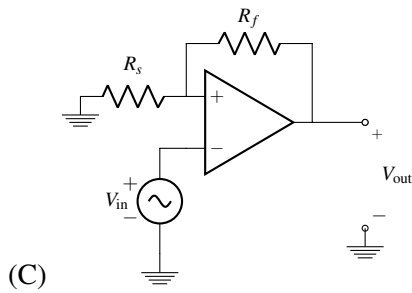
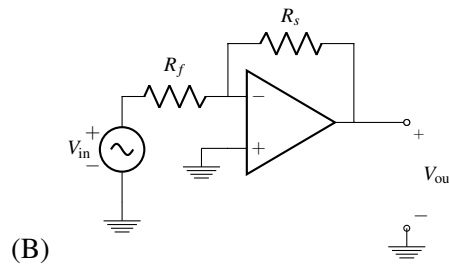
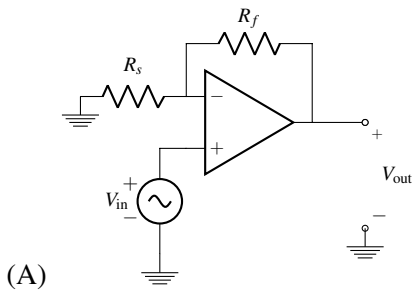
By inspecting the equation for R_t , you can determine that a lower temperature will result in a higher value of R_t . Therefore, in order for the thermostat to be set to temperatures only lower than or equal to 85°F , R_v should be restricted to resistances greater than or equal to $3.8\text{ k}\Omega$.

11. Op Amp Drills (26 points)

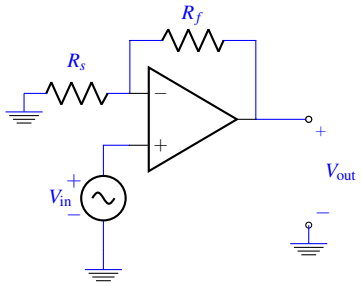
Congratulations! Fresh off your EECS 16A experience you have been hired as an intern at Linear Circuits, Inc. to design next generation systems. Your first task will be to come up with a circuit that can perform linear operations to received signals of interest. Specifically, you want to build a circuit whose output is a weighted sum of multiple received inputs, i.e. $V_{out} = \alpha V_{in,1} + \beta V_{in,2} + \gamma V_{in,3} + \dots$, with the coefficients $\alpha, \beta, \gamma \in \mathbb{R}$.

To do so you will be using your favorite circuit element, the op amp! As usual with circuit design, you decide to start simple and then combine your fundamental building blocks to achieve more complicated functionality.

- (a) (3 points) Which of the following op amp configurations would you use in order to get an input-output relationship of the form: $V_{out} = (1 + \frac{R_f}{R_s})V_{in}$?

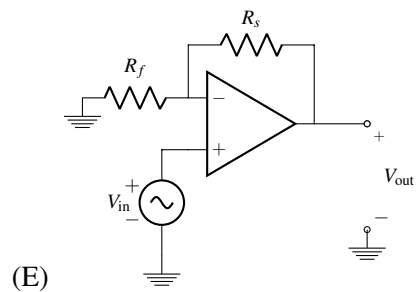
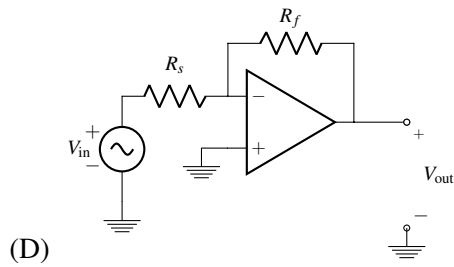
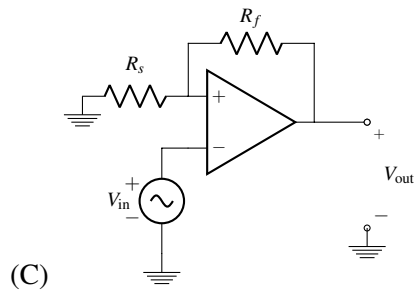
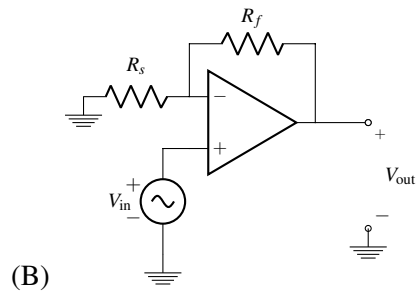
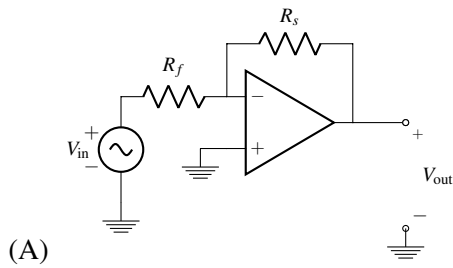


Solution:

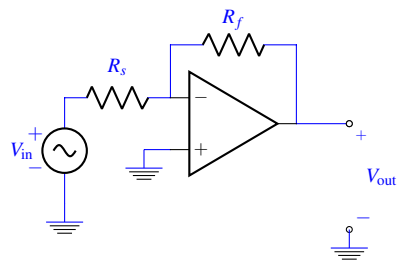


The input - output relationship we are looking for in this case is the one of the non-inverting amplifier. By pattern matching we get that the above topology is identical to the non-inverting amplifier, with R_f connected between the output of the opamp and its “-” terminal, R_s connected between the “-” terminal of the opamp and ground, and the input applied to the “+” terminal.

- (b) (3 points) The circuit from part (a) can only multiply the input by positive numbers, and your boss tells you that you need to implement negative coefficients as well. Which of the following configurations results in $V_{out} = -\frac{R_f}{R_s} V_{in}$?

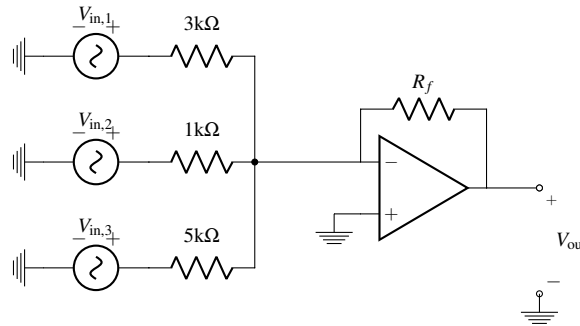


Solution:

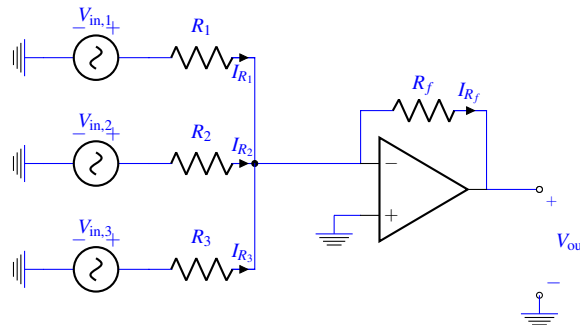


Again, by pattern matching we see that the above circuit is identical to the inverting amplifier that was presented in lecture and discussion.

- (c) (4 points) Now that you have both positive and negative coefficients, your next step is to combine multiple inputs into one output, using the following circuit. Express V_{out} in terms of $V_{in,1}$, $V_{in,2}$, $V_{in,3}$, and R_f .



Solution: This circuit is the inverting summer which was also presented in lecture. Let's analyze it again.



After labeling currents on the circuit diagram we will write a KCL equation on node u^- :

$$I_{R_1} + I_{R_2} + I_{R_3} = I_{R_f}$$

$$\frac{V_{R_1}}{R_1} + \frac{V_{R_2}}{R_2} + \frac{V_{R_3}}{R_3} = \frac{V_{R_f}}{R_f}$$

Because of GR #2 we have that $u^- = u^+ = 0$, so the element voltage can be written as:

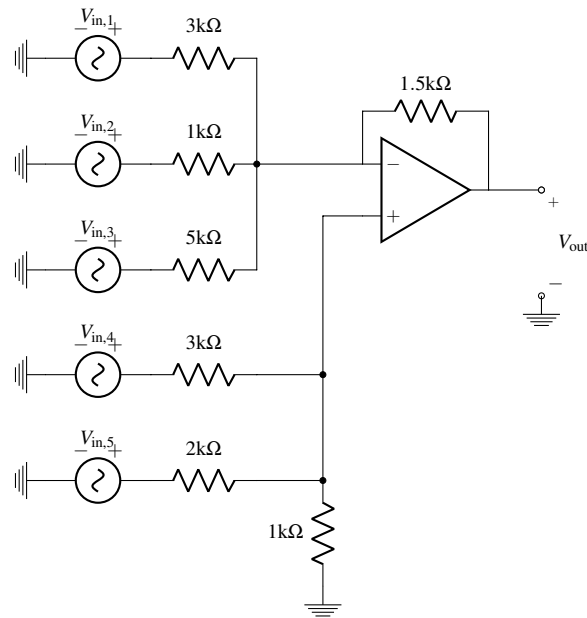
$$\frac{V_{in,1} - 0}{R_1} + \frac{V_{in,2} - 0}{R_2} + \frac{V_{in,3} - 0}{R_3} = \frac{0 - V_{out}}{R_f}$$

$$V_{out} = -\frac{R_f}{R_1}V_{in,1} - \frac{R_f}{R_2}V_{in,2} - \frac{R_f}{R_3}V_{in,3}$$

$$V_{out} = -\frac{R_f}{1k\Omega}V_{in,2} - \frac{R_f}{5k\Omega}V_{in,3} - \frac{R_f}{3k\Omega}V_{in,1}$$

Notice, superposition also gives the same result, since when all sources but one source are nulled the circuit is simplified to the inverting amplifier from the part b. (The resistors associated with the nulled sources are connected to ground on their "left" terminal - since we replace their source with a wire - and to u^- on the right, but because of GR #2, $u^- = u^+ = 0$, so we can neglect those).

- (d) (4 points) However, your boss points out that your design above doesn't allow for a mixture of positive and negative coefficients. Determined to succeed, you design the following circuit. What is the output of your new design as a function of the input voltages $V_{in,1}$, $V_{in,2}$, ..., $V_{in,5}$?



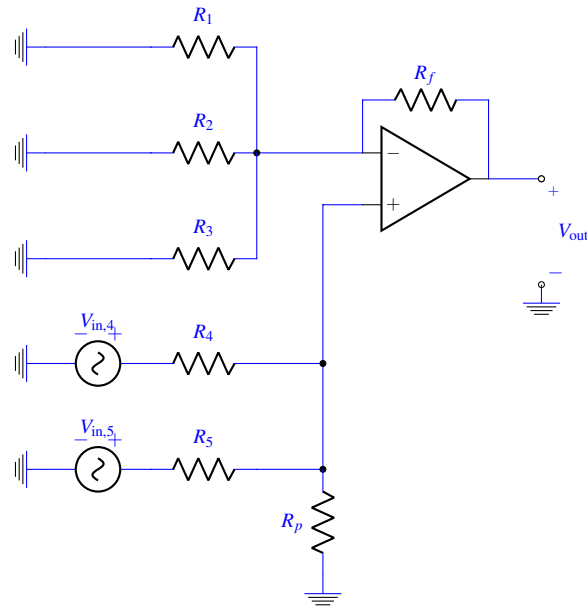
Solution:

In this problem the easiest way to get to the solution algebraically is to apply superposition looking separately at the 3 sources connected to the inverting terminal of the op amp, u^- and at the 2 sources connected to the non-inverting terminal of the op amp, u^+ . Nulling the 2 sources connected to the non-inverting terminal of the op amp we get an identical topology to the one we had in part c). (The resistors associated with the nulled sources can be combined in one equivalent resistance with one terminal connected to ground and the other to u^+ . Because GR #1 applies, no current can be flowing through that resistor. Hence the voltage drop across it has to be zero and $u^+ = 0$ as well. This means we have the same configuration as in part c).

Copying the result from part c here we have:

$$V_{out,inv} = -\frac{R_f}{R_1}V_{in,1} - \frac{R_f}{R_2}V_{in,2} - \frac{R_f}{R_3}V_{in,3}$$

Now let's look at the circuit we get when the 3 sources connected to the inverting terminal of the op amp are nulled:



To calculate u^+ we can use superposition for the two sources and the voltage divider formula:

$$u_+ = \frac{R_p || R_5}{R_4 + R_p || R_5} V_{in,4} + \frac{R_p || R_4}{R_5 + R_p || R_4} V_{in,5}$$

Now notice that once we find the voltage at u^+ we can apply the non-inverting amplifier formula $(1 + \frac{R_{top}}{R_{bot}})$ with $R_{bot} = R_1 || R_2 || R_3$, and $R_{top} = R_f$.

$$V_{out,non-inv} = \left(1 + \frac{R_f}{R_1 || R_2 || R_3}\right) \frac{R_p || R_5}{R_4 + R_p || R_5} V_{in,4} + \left(1 + \frac{R_f}{R_1 || R_2 || R_3}\right) \frac{R_p || R_4}{R_5 + R_p || R_4} V_{in,5}$$

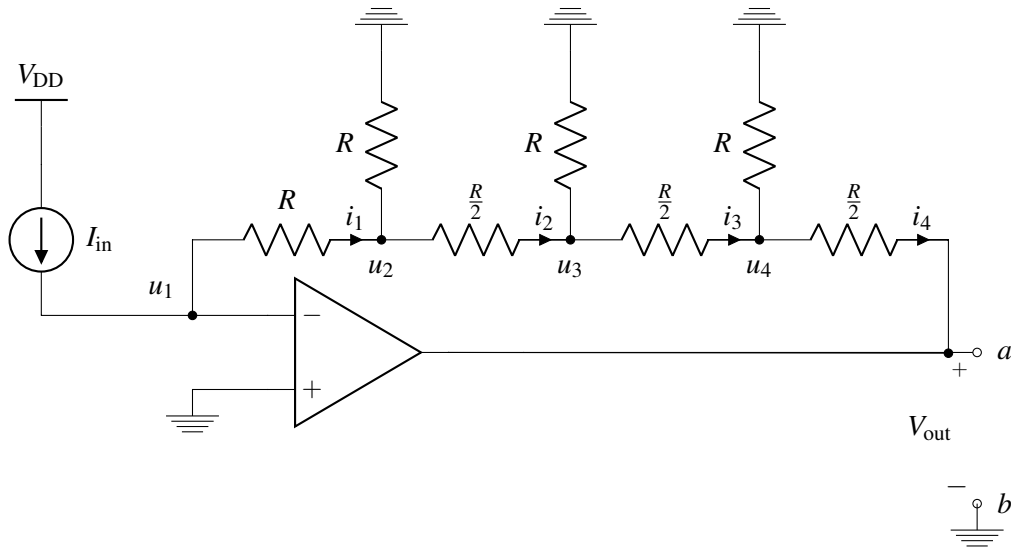
Lastly, we can find the overall output by combining the two previous results:

$$V_{out} = V_{out,inv} + V_{out,non-inv}$$

$$V_{out} = -\frac{R_f}{R_1} V_{in,1} - \frac{R_f}{R_2} V_{in,2} - \frac{R_f}{R_3} V_{in,3} + \left(1 + \frac{R_f}{R_1 || R_2 || R_3}\right) \frac{R_p || R_5}{R_4 + R_p || R_5} V_{in,4} + \left(1 + \frac{R_f}{R_1 || R_2 || R_3}\right) \frac{R_p || R_4}{R_5 + R_p || R_4} V_{in,5}$$

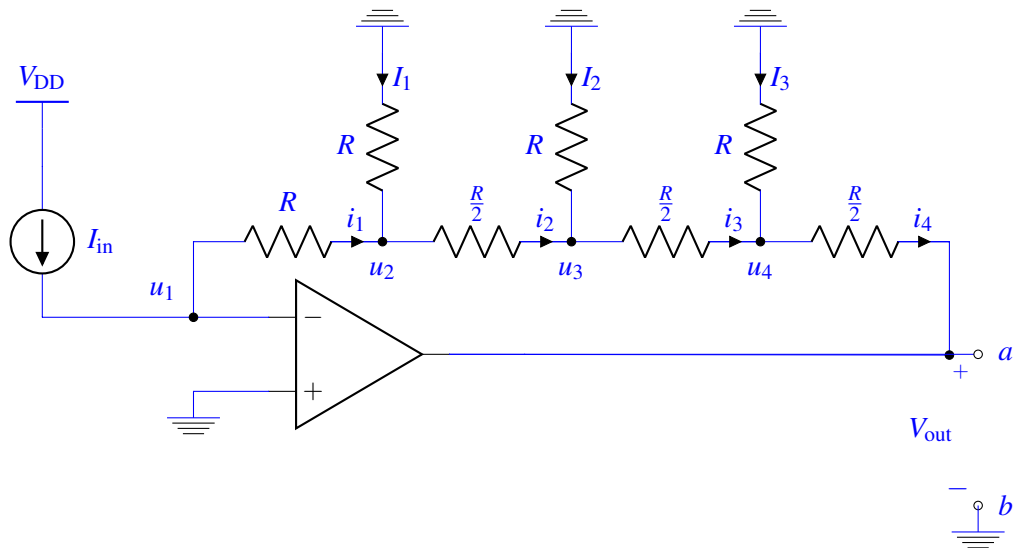
$$V_{out} = -3.833 V_{in,1} - 2.875 V_{in,2} - 5.75 V_{in,3} + 0.6 V_{in,4} + 0.9 V_{in,5}$$

After successfully tackling the previous task and creating a weighted voltage summer, your mentor presents you with another problem. Your job will be to analyze the following circuit. Your mentor claims that you can use this circuit to convert an input current to an output voltage.



(e) (4 points) To verify his claim, analyze the circuit and calculate the currents labeled i_1, i_2, i_3, i_4 , and the output voltage V_{out} . What are their values?

Solution:



Let's write GR #2 and a KCL equation for every node apart from V_{out} :

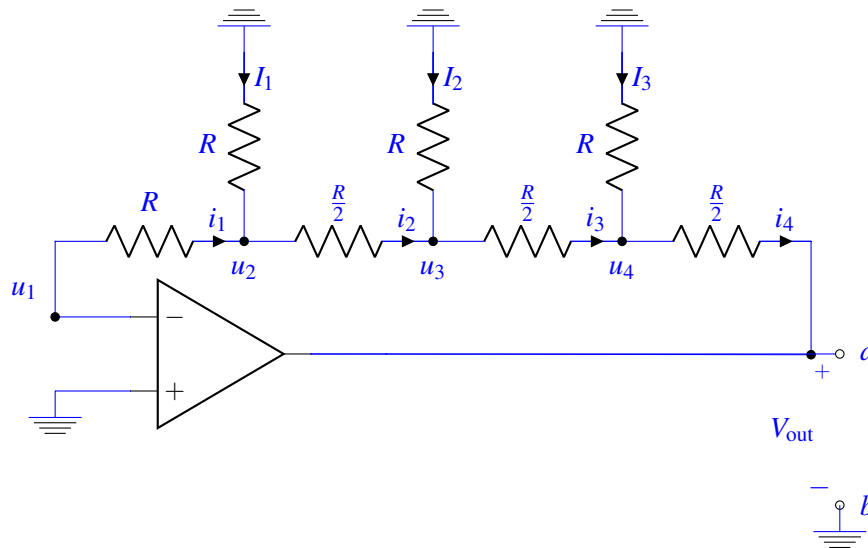
$$\begin{aligned}
 u_1 = u^- = u^+ = 0 & \quad (\text{GR \#2}) \\
 I_m = i_1 + i^- = i_1 + 0 & \quad (\text{GR \#1}) \\
 i_1 + I_1 = i_2 & \quad (\text{node } u_2) \\
 i_2 + I_2 = i_3 & \quad (\text{node } u_3) \\
 i_3 + I_3 = i_4 & \quad (\text{node } u_4)
 \end{aligned}$$

The fastest way to tackle this problem is to sequentially calculate the currents and voltages from the input to the output:

$$\begin{aligned}
 i_1 &= I_{in} \\
 u_2 &= u_1 - i_1 R = 0 - I_{in} R = -I_{in} R \\
 I_1 &= \frac{0 - u_2}{R} = I_{in}, \quad i_2 = i_1 + I_1 = 2I_{in} \\
 u_3 &= u_2 - i_2 \frac{R}{2} = -I_{in} R - 2I_{in} \frac{R}{2} = -2I_{in} R \\
 I_2 &= \frac{0 - u_3}{R} = 2I_{in}, \quad i_3 = i_2 + I_2 = 4I_{in} \\
 u_4 &= u_3 - i_3 \frac{R}{2} = -2I_{in} R - 4I_{in} \frac{R}{2} = -4I_{in} R \\
 I_3 &= \frac{0 - u_4}{R} = 8I_{in}, \quad i_4 = i_3 + I_3 = 8I_{in} \\
 V_{out} &= u_4 - i_4 \frac{R}{2} = -4I_{in} R - 8I_{in} \frac{R}{2} = -8I_{in} R
 \end{aligned}$$

- (f) (4 points) What is the Thevenin equivalent voltage and the Thevenin equivalent resistance between terminals a and b in the circuit above?

Solution: The Thevenin equivalent voltage is equal to V_{out} from the previous subpart, $V_{th} = V_{out} = -8I_{in}R$. To calculate R_{th} we need to zero out the current source input (replace it with an open circuit):



Still, the circuit is in NFB, so by GR #2 we will have that $u^- = u^+ = 0V$.

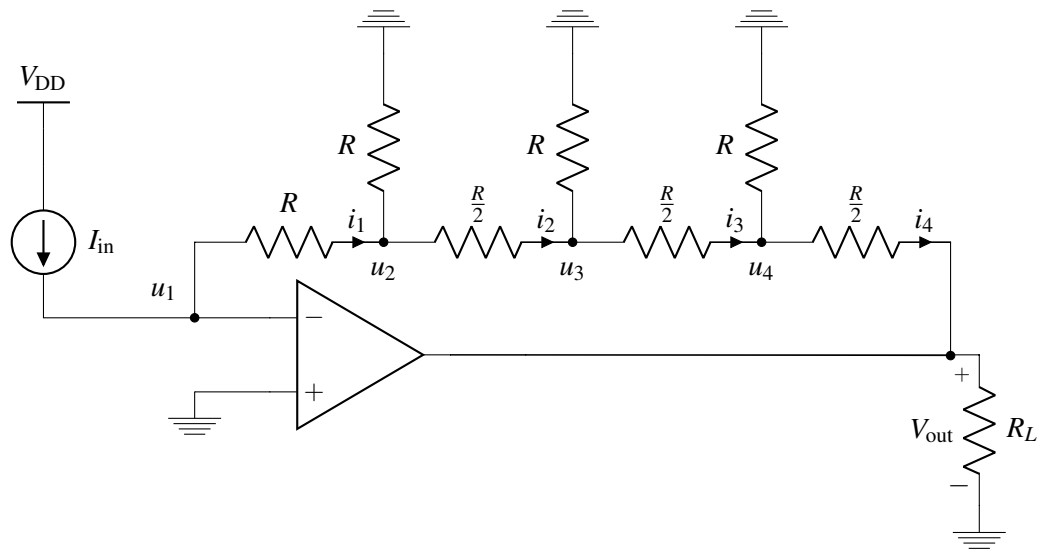
Before applying a test source, we can see that because of GR #1, i_1 has to be zero.

This in turn means that there will be no voltage drop across the leftmost R , which implies that $u_2 = u_1 = 0$. Substituting in the equations from the previous part we will get that $V_{out} = 0V$ as well. This means that the resistive network can be effectively ignored, and we will only “see” at the equivalent resistance of the voltage controlled voltage source modeling the op amp, which is 0.

Another way to look at this is that we will have the equivalent resistance of the voltage controlled voltage source modeling the op amp in parallel with the resistance looking into the resistive network. This will effectively be a wire in parallel with some resistance (since the equivalent resistance of a voltage source is a wire) which is $0 || R_{eq} = 0$.

(g) (4 points) As is the case in most real-world applications, you want to use this incoming signal in order to drive a load that will actuate something. That “something” can be a speaker, a motor, or a heater among other things.

Which of the quantities you calculated in part (e) ($i_1, i_2, i_3, i_4, V_{out}$), if any, will change if you connect a load resistance as shown in the figure below?



Solution: Since the output of the op amp is set by a voltage controlled voltage source, it will maintain its value regardless of the load attached to it. To do so, it will provide any additional current necessary.

12. MP3 Player (18 points)

Smartphones store songs as a sequence of binary numbers (0s or 1s) called “bits” that must be converted to analog voltages before the song is played through a headset or speaker. The circuits that achieve this are called “Digital to Analog Converters”, or DACs for short. Let’s design a DAC!

(a) (4 points) You build the following 4-bit DAC:

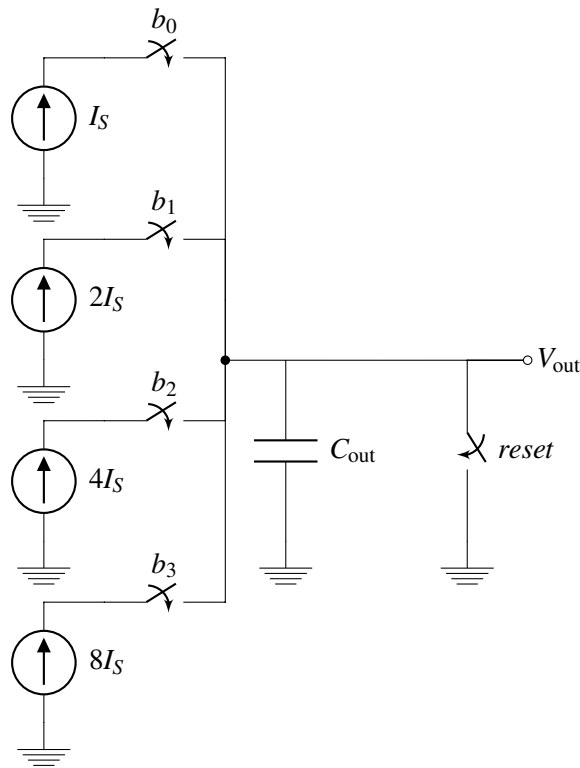


Figure 5: Current Source 4-bit DAC circuit

You circuit converts a sequence of 4 bits to a voltage as follows: Initially, the capacitor, C_{out} , is discharged, so $V_{out}(0) = 0$. Then, with the *reset* switch open, the switches $b_0 - b_3$ are controlled by the input bit sequence: If bit b_i has a value of “1” then the corresponding switch is closed; if it has a value of “0” the switch is open. After a fixed amount of time, t_{charge} , all the b_i switches are opened, and the output voltage, $V_{out}(t_{charge})$, is measured.

What is the value of C_{out} that makes the largest possible output voltage, $V_{out,max}(t_{charge})$, equal to 3V? Let $t_{charge} = 20\mu s$ and $I_S = 2\mu A$.

Disclaimer: Normally, open-circuiting a current source (which happens here when one of the switches b_i is open) can be dangerous. In this problem, please assume that the current source is automatically shut off when connected to an open circuit.

Solution: The maximum output voltage will occur if all bits are “1”, in which case the capacitor C_{out} will be charged by a current $I = 15I_S$

The current and the derivative of voltage on a capacitor are related as follows:

$$I_s = C_{out} \frac{dV_{out}}{dt}$$
$$C_{out} = \frac{15I_s}{V_{out}(t_{charge}) - V_{out}(0)} t_{charge}$$

Which after substitution for this example gives: $C_{out} = 200\text{pF}$.

- (b) (4 points) You show your circuit to your TA, Ben, who reminds you that it's really hard to build a current source. Luckily for you, Ben is very resourceful and provides you with a circuit of his own. His DAC uses capacitors sharing charge to produce different voltages.

To remind you how this idea works he tells you to analyze the circuit in Figure 6. For time $t < 0$, the switch is open and the capacitors are charged to voltages V_1 and V_2 , respectively. At time $t = 0$ the switch is closed. What is the voltage V_1 after the charges have redistributed?

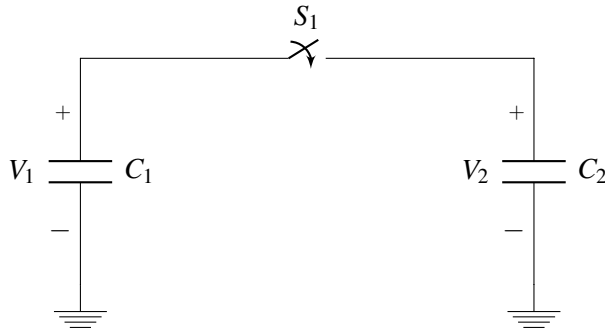


Figure 6: Capacitor Charge Sharing

Use the following values: $C_1 = 4\text{F}$, $C_2 = 8\text{F}$, $V_1 = 3\text{V}$, $V_2 = 6\text{V}$.

Solution: After time, $t > 0$ we will have that the two capacitors are connected in parallel with their bottom node at ground and their top node floating. Hence, the total charge on that node has to be conserved. Equating the total charge stored on the top plates of the two capacitors before and after $t = 0$ we get:

$$C_1 V_1 + C_2 V_2 = C_1 V_{1,t>0} + C_2 V_{1,t>0}$$

$$V_{1,t>0} = \frac{C_1 V_1 + C_2 V_2}{C_1 + C_2}$$

Substituting for this example we get: $V_{1,t>0} = \frac{60}{12}\text{V}$

Following Ben's advice, you build a full DAC, shown in Figure 7. It operates in two phases and is controlled by a bit signal b , which can be 0 or 1. The table below indicates the state of each switch for both phases.

Switch	Phase 1	Phase 2
S_1	closed if $b = 1$, open otherwise	open
S_2	closed if $b = 0$, open otherwise	open
S_3	open	closed

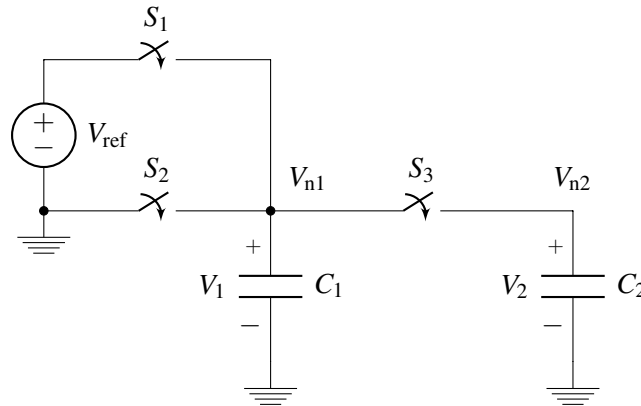
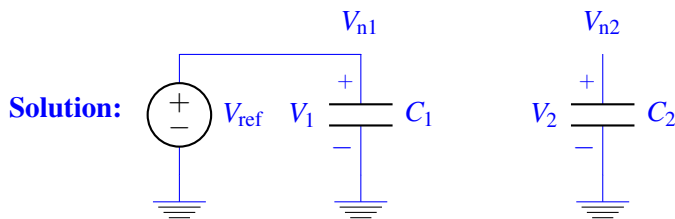
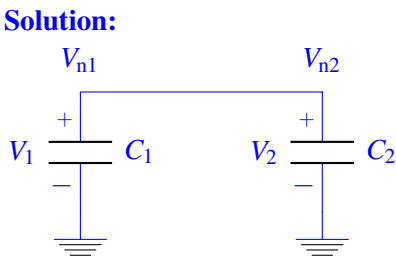


Figure 7: DAC Circuit Diagram

(c) (3 points) Draw the circuit that corresponds to the DAC circuit diagram (Figure 7) during **Phase 1** when $b = 1$.



(d) (3 points) Draw the circuit that corresponds to the DAC circuit diagram (Figure 7) during **Phase 2** when $b = 1$.



- (e) (4 points) The circuit repeatedly cycles through Phases 1 and 2. In each step, the value of the control signal b represents one “bit” of the number to be converted. Given that $C_1 = C_2$, fill in the values of V_{n1} (voltage of C_1 measured in Phase 1) and V_{n2} (voltage of C_2 measured in Phase 2) in the table below. The first two rows are filled in for illustration. Assume C_2 is initially discharged at the beginning of Step 1.

Step	b	V_{n1} in Phase 1	V_{n2} in Phase 2
1	0	0V	0V
2	1	V_{ref}	$\frac{1}{2}V_{ref}$
3	1	a	b
4	1	c	d

Solution:

As the circuit switches between phase 1 and 2 multiple times, the output voltage V_{n2} at step k is going to be given by applying charge conservation for the previous step $k - 1$: The only difference between here and part b is that we are looking into $k - 1, k$, instead of $t < 0, t \geq 0$. This leads to the following equation:

$$V_{n2,k+1} = \frac{C_1 V_{n1,k} + C_2 V_{n2,k}}{C_1 + C_2}$$

And the voltage V_{n1} at time k only depends on the value of the current bit b_k with:

$$V_{n1,k} = \begin{cases} V_{ref}, & \text{if } b = 1 \\ 0, & \text{if } b = 0 \end{cases}$$

Filling out the table one step at a time we get to the solution:

$$a = V_{ref}, b = \frac{3}{4}V_{ref}, c = V_{ref}, d = \frac{7}{8}V_{ref}$$