RC Circuits / Differential Equations

OUTLINE
• Review: CMOS logic circuits & voltage signal propagation
• Model: RC circuit → differential equation for $V_{out}(t)$
• Derivation of solution for $V_{out}(t)$ → propagation delay formula

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Meet the Guest Lecturer

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• Joined UCB EECS faculty in 1996
• Courses taught: 40, 105, 130, 143, 290D, 375
• Research in nanoelectronic & nanomechanical devices
The MOSFET

- Current flowing between the heavily doped SOURCE & DRAIN regions is controlled by the voltage on the GATE electrode.
- N-channel & P-channel MOSFETs operate in a complementary manner.

CIRCUIT SYMBOLS:

<table>
<thead>
<tr>
<th>NMOSFET</th>
<th>PMOSFET</th>
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<tr>
<td><img src="image1" alt="NMOSFET Circuit Symbol" /></td>
<td><img src="image2" alt="PMOSFET Circuit Symbol" /></td>
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The CMOS Inverter

- Low static power consumption, since one transistor is always off in steady state.

CIRCUIT

- ![CMOS Inverter Circuit](image3)

SWITCH MODELS

- ![Switch Model N-channel](image4)
- ![Switch Model P-channel](image5)
Pull-Down and Pull-Up Devices

- In CMOS logic gates, NMOS transistors are used to connect the output to GND, whereas PMOS transistors are used to connect the output to \( V_{DD} \).
  - An NMOS transistor functions as a **pull-down device** when it is turned on (gate voltage = \( V_{DD} \)).
  - A PMOS transistor functions as a **pull-up device** when it is turned on (gate voltage = GND).

Voltage Signal Propagation

- When an input voltage of a logic gate is changed, there is a **propagation delay** before the output of the logic gate changes, due to capacitive loading at the output.

Propagation delay is measured between the 50% transition points of the input and output signals.
**RC Circuit Model for High-Low Transition**

Initially $V_{out} = V_{DD}$; then NMOSFET(s) connect(s) $V_{out}$ to GND:

- Pull-up network is modeled as an open switch
- Pull-down network is modeled as a resistor

$$\dot{V}_{out} = -RC_{L} \frac{dV_{out}}{dt} - i(t)$$

$$i(t) = \frac{V_{out}}{R_{ON,N}}$$

**Output Load Capacitance of a Logic Gate**

- The output load capacitance of a logic gate comprises several components:
  - pn-junction capacitance for both NMOS and PMOS transistors
  - capacitance of connecting wires
  - input capacitances of the “fan-out” gates

$$C_{gate,N}, C_{gate,P}$$
**Derivation of RC Model**

\[
\begin{align*}
V_{\text{out}} & = V_{\text{po}} \\
\frac{\text{d}V_{\text{out}}}{\text{d}t} & = i_C + \frac{1}{C_{\text{out}}} \frac{\text{d}V_{\text{out}}}{\text{d}t}
\end{align*}
\]

\[
i_C = C_{\text{gd}p} \frac{\text{d}V_{\text{out}}}{\text{d}t} + C_{\text{gd}p} \frac{\text{d}V_{\text{out}}}{\text{d}t}
\]

\[
i_\text{c} = C_{\text{gd}p} \frac{\text{d}V_{\text{out}}}{\text{d}t} + C_{\text{gd}p} \frac{\text{d}V_{\text{out}}}{\text{d}t}
\]

\[
\Rightarrow i_C = \left( C_{\text{gd}p} + C_{\text{gd}p} \right) \frac{\text{d}V_{\text{out}}}{\text{d}t}
\]

\[
\Rightarrow \frac{\text{d}V_{\text{out}}}{\text{d}t} = \frac{-i_C}{C_L} + \frac{1}{C_L} \frac{\text{d}V_{\text{out}}}{\text{d}t}
\]

**Derivation of \( V_{\text{out}}(t) \) for High-Low Transition**

Approach #1: By separation of variables

\[
\frac{\text{d}t}{\text{d}V_{\text{out}}} = -RC \Rightarrow \int \frac{1}{V_{\text{out}}} \text{d}V_{\text{out}} = \int -\frac{1}{RC} \text{d}t
\]

\[
\Rightarrow t + C_1 = -RC \ln V_{\text{out}} \Rightarrow \frac{t}{RC} + \frac{C_1}{RC} = \ln V_{\text{out}}
\]

\[
\Rightarrow V_{\text{out}} = e^{\frac{t}{RC} + \frac{C_1}{RC}} = e^{e^{-t/RC}} -t/RC
\]

**Initial Condition:** \( t = 0, V_{\text{out}} = V_{\text{po}} = C \)

\[
V_{\text{out}}(t) = V_{\text{po}} e^{-t/RC}
\]
**Derivation of** $V_{out}(t)$ **for High-Low Transition**

Approach #2: With eigenfunctions

\[
V_{out} = -RC f(V_{out})
\]

\[-\frac{1}{RC} V_{out} = f(t_{out}) \rightarrow V_{out} \text{ is an eigenfunction of } f(t)\]

Only an exponential function has a derivative proportionate to itself

\[\rightarrow V_{out} = Ke^{t/\tau} \quad \text{where } \tau \text{ is a constant, } \text{“time constant”}\]

\[\text{Plugging Diff. Eqn.: } Ke^{t/\tau} = -RC \frac{d}{dt}(Ke^{t/\tau}) = -RC (\frac{t}{\tau})e^{t/\tau}\]

\[\Rightarrow -\frac{RC}{\tau} = 1 = \tau = RC \quad V_{out} = Ke^{t/\tau} = V_{DD} e^{-t/RC}\]

**Derivation of Formula for** $t_{pHL}$

\[V_{out}(t) = V_{DD} e^{-t/RON.N.C_L}\]

At $t = t_{pHL}$:

\[V_{out} = \frac{V_{DD}}{2} = V_{DD} e^{-t_{pHL}/RC}\]

\[\frac{1}{2} = e^{-t_{pHL}/RC} \Rightarrow 2 = e^{t_{pHL}/RC}\]

\[\ln(2) = t_{pHL}/RC\]

\[\Rightarrow t_{pHL} = RC \ln(2) = 0.69 RC\]
RC Circuit Model for Low-High Transition

Initially $V_{out} = 0$; then PMOSFET(s) connect(s) $V_{out}$ to $V_{DD}$:

- Pull-up network is modeled as a resistor:
  $$i(t) = \frac{V_{DD} - V_{out}}{R_{ON,P}}$$

- Pull-down network is modeled as an open switch:
  $$i = \frac{V_{DD} - V_{out}}{R_{OFF,P}} = C_L \frac{dV_{out}}{dt}$$

$$V_{DD} - V_{out} = R_{ON,P} C_L \frac{dV_{out}}{dt}$$

Derivation of RC Model

Redraw:

Solution to Diff Eqn is the same as before, since $$\frac{dV_{out}}{dt} = \frac{d(V_{out} - V_{DD})}{dt}$$
**Derivation of $V_{out}(t)$ for Low-High Transition**

Initially, $V_{out} = 0$ and $V'_{out} = 0 - V_{DD} = -V_{DD}$

$$V_{out}' = V_{out}(t=0) e^{-t/R_{in,p} C_L}$$

$$V_{out} - V_{DD} = -V_{DD} e^{-t/R_{in,p} C_L}$$

$$V_{out} = V_{DD} \left[1 - e^{-t/R_{in,p} C_L}\right]$$

**Derivation of Formula for $t_{PLH}$**

$$V_{out}(t) = V_{DD} \left(1 - e^{-t/R_{ox,p} C_L}\right)$$

At $t = t_{PLH}$:

$$V_{out} = \frac{V_{DD}}{2} = V_{DD} \left(1 - e^{-t_{PLH}/R_C}\right)$$

$$e^{-t_{PLH}/R_C} = \frac{1}{2} = e^{t_{PLH}/R_C} = 2$$

$$t_{PLH}/R_C = \ln(2) \Rightarrow t_{PLH} = \frac{\ln(2)}{R_C} = 0.69 R_C$$
Minimizing Propagation Delay

A fast CMOS logic circuit is built by

1. **Keeping the output capacitance** $C_L$ **small**
   - Minimize the area of drain pn junctions.
   - Lay out devices to minimize interconnect capacitance.
   - Avoid large fan-out.

2. **Decreasing the equivalent resistance of the transistors**
   - Decrease gate length $L_G$
   - Increase transistor width $W$
   - ... but this increases pn junction area and hence $C_L$

3. **Increasing $V_{DD}$**
   - trade-off with power consumption…

Classroom Analogy