RC Circuits / Differential Equations

OUTLINE

- Review: CMOS logic circuits & voltage signal propagation
- Model: *RC* circuit → differential equation for $V_{out}(t)$
- Derivation of solution for $V_{out}(t)$ → propagation delay formula

EE16B, Fall 2015

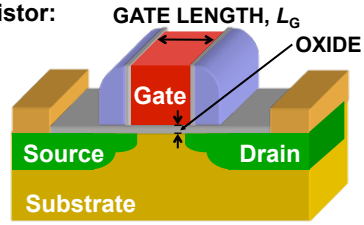
Meet the Guest Lecturer

Prof. Tsu-Jae King Liu

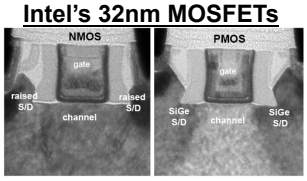
- Joined UCB EECS faculty in 1996
- Courses taught: 40, 105, 130, 143, 290D, 375
- Research in nanoelectronic & nanomechanical devices

The MOSFET

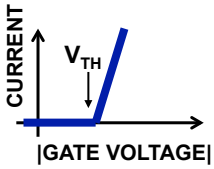
Metal-Oxide-Semiconductor Field-Effect Transistor:



Intel's 32nm MOSFETs

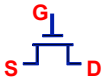


- **Current flowing between the heavily doped SOURCE & DRAIN regions is controlled by the voltage on the GATE electrode**
- **N-channel & P-channel MOSFETs operate in a complementary manner**

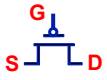


CIRCUIT SYMBOLS:

NMOSFET



PMOSFET



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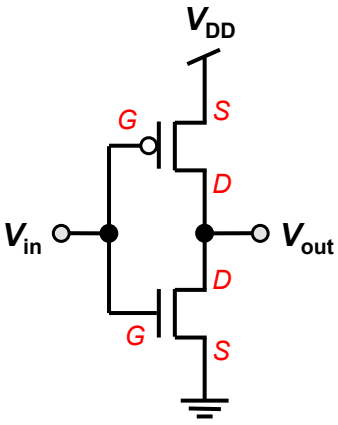
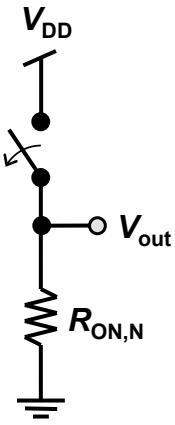
The CMOS Inverter

CIRCUIT

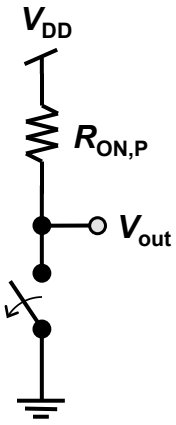


✓ **Low static power consumption, since one transistor is always off in steady state**

SWITCH MODELS



$V_{IN} = V_{DD}$



$V_{IN} = 0$ V

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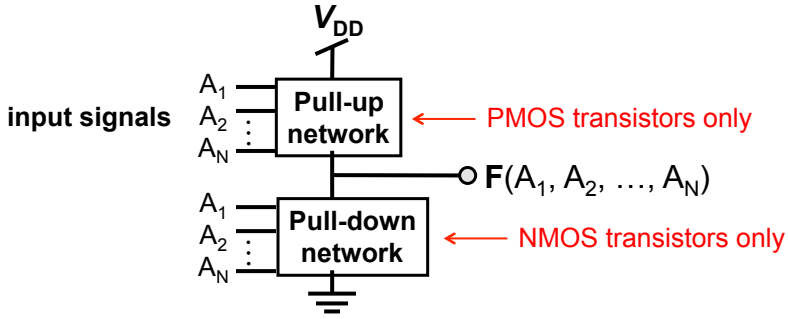
Pull-Down and Pull-Up Devices

- In CMOS logic gates, NMOS transistors are used to connect the output to **GND**, whereas PMOS transistors are used to connect the output to V_{DD}.
  - An NMOS transistor functions as a ***pull-down device*** when it is turned on (gate voltage = V_{DD})
  - A PMOS transistor functions as a ***pull-up device*** when it is turned on (gate voltage = **GND**)



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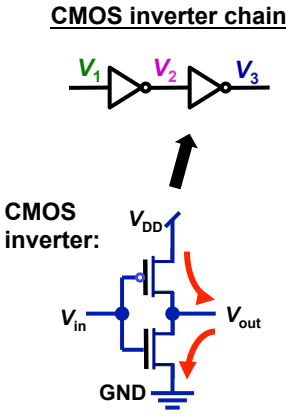
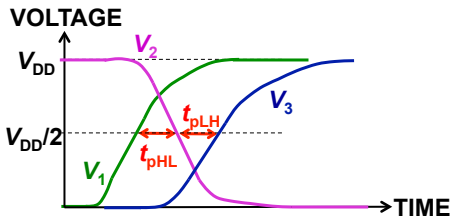
Voltage Signal Propagation

- When an input voltage of a logic gate is changed, there is a ***propagation delay*** before the output of the logic gate changes, due to capacitive loading at the output.





Propagation delay is measured between the 50% transition points of the input and output signals.

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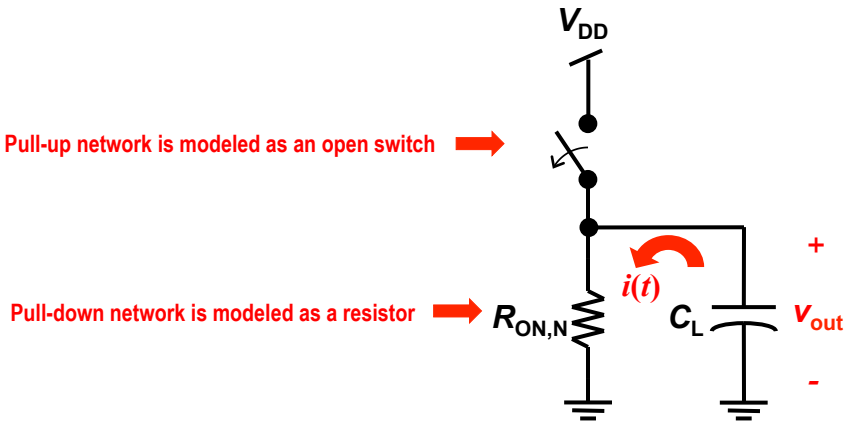
RC Circuit Model for High-Low Transition

Initially $V_{out} = V_{DD}$; then NMOSFET(s) connect V_{out} to GND:



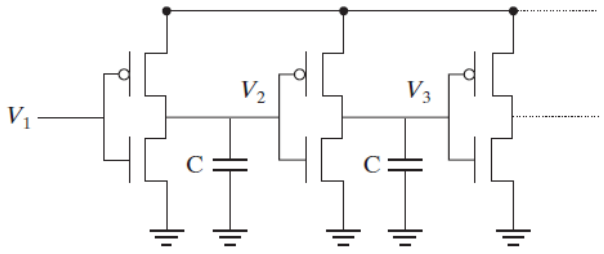
$$v_{out} = -R_{ON,N} C_L \, dv_{out}/dt$$

Output Load Capacitance of a Logic Gate

- **The output load capacitance of a logic gate comprises several components:**

"intrinsic capacitance" →
- **pn-junction capacitance**
  for both NMOS and PMOS transistors

"extrinsic capacitance"
- **capacitance of connecting wires**
- **input capacitances of the "fan-out" gates**
  $C_{gate,N}$, $C_{gate,P}$



Derivation of RC Model

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Derivation of $V_{out}(t)$ for High-Low Transition

By separation of variables:

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Derivation of $V_{out}(t)$ for High-Low Transition

With eigenfunctions:

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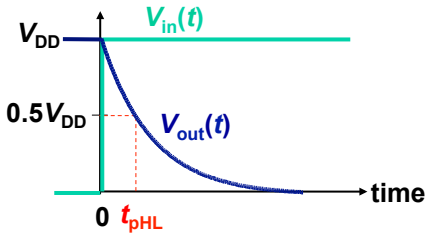
Derivation of Formula for t_{pHL}

$$V_{out}(t) = V_{DD} e^{-t/R_{ON,N}C_L}$$



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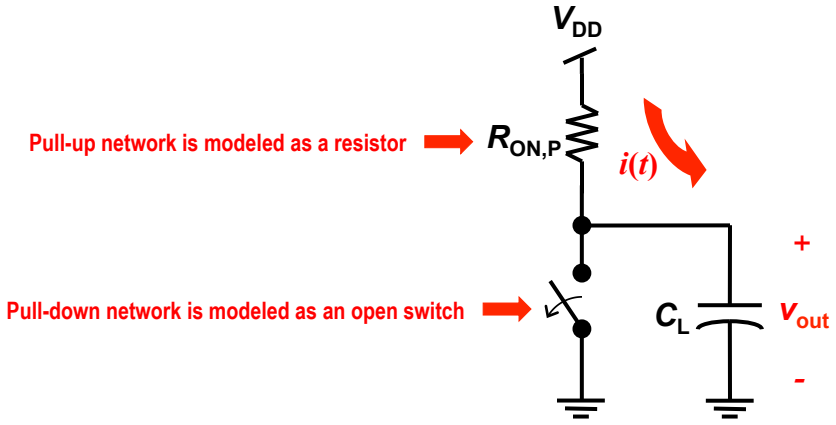
RC Circuit Model for Low-High Transition

Initially V_{out} = 0; then PMOSFET(s) connect V_{out} to V_{DD}:



$$V_{DD} - v_{out} = -R_{ON,P} C_L \, dv_{out}/dt$$

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Derivation of $V_{out}(t)$ for Low-High Transition

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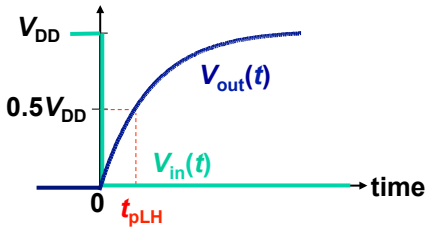
Derivation of Formula for t_{pLH}

$$V_{out}(t) = V_{DD}\left(1 - e^{-t/R_{ON,P}C_L}\right)$$



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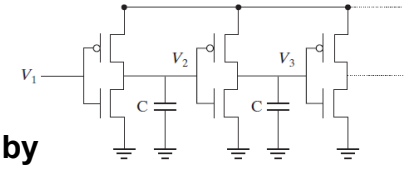
Minimizing Propagation Delay



A fast CMOS logic circuit is built by

1. **Keeping the output capacitance C_L small**
   - → Minimize the area of drain pn junctions.
   - → Lay out devices to minimize interconnect capacitance.
   - → Avoid large fan-out.
2. **Decreasing the equivalent resistance of the transistors**
   - → Decrease gate length L_G
   - → Increase transistor width W
     … but this increases pn junction area and hence C_L
3. **Increasing V_{DD}**
   - → trade-off with power consumption…

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Classroom Analogy