EECS 16B Designing Information Devices and Systems II
Fall 2016 Murat Arcak and Michel Maharbiz

Homework 1

This homework is due September 5, 2016, at Noon.

1. Homework process and study group

(a) Who else did you work with on this homework? List names and student ID's. (In case of hw party, you can also just describe the group.)

(b) How long did you spend working on this homework? How did you approach it?

2. Complex Numbers 1

Let complex numbers z_1 and z_2 be defined as follows:

$$z_1 = 6 - j4$$
$$z_2 = -2 + j$$

(a) Express z_1 and z_2 in polar form.

(b) Determine $|z_1|$.

(c) Determine the product $z_1 z_2$ in polar form.

(d) Determine the ratio z_1/z_2 in polar form.

(e) Determine z_1^2 and compare it to $|z_1|^2$.

(f) Determine $z_1/(z_1 - z_2)$.

3. Complex Numbers 2

Consider the complex number $z = -8 + 6j$. Determine the following quantities:

(a) $|z|^2$

(b) z^2 in polar form

(c) $1/z$ in polar form

(d) z^{-3} in polar form

(e) $\Re(1/z^2)$

(f) $\Im(z^*)$

(g) $\Im[(z^*)^2]$

(h) $\Re[(z^*)^{-1/2}]$

4. Complex Numbers 3

Consider the complex number $z = e^{j\omega t}$ where ω is a known constant.

(a) Express z in rectangular coordinates.

(b) Draw z in the complex plane for $t = \frac{\pi}{4\omega}$.

(c) Draw z in the complex plane for $t = \frac{\pi}{2\omega}$.

(d) Draw z in the complex plane for $t = \frac{5\pi}{4\omega}$.

(e) Draw z in the complex plane for $t = \frac{7\pi}{4\omega}$.

(f) Draw z in the complex plane for $t = \frac{9\pi}{4\omega}$.

(g) Plot $\Re(z)$ for $t = \frac{\pi}{4\omega}, \frac{\pi}{2\omega}, \frac{5\pi}{4\omega}, \frac{7\pi}{4\omega}, \frac{9\pi}{4\omega}$ What does this function remind you of?

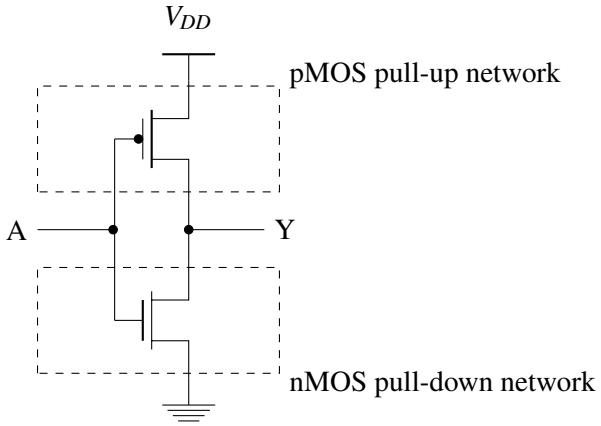
(h) Is $z(t)$ periodic?

(i) What is $\Re(e^{j(\omega t+\phi)})$? What is ϕ called in the resulting function?

5. Transistors and Boolean Logic

A Boolean formula can be implemented in digital circuitry using nMOS and pMOS transistors. In circuits, the truth value 1 (*true*) is represented by a high voltage, called POWER (V_{DD}). The truth value 0 (*false*) is represented by a low voltage, called GROUND (GND). In this problem, we will only use the truth values in order to simplify notations. That is, if you see $A = 1$ for a point A, then it means the voltage of A is equal to V_{DD}. Similarly, if $A = 0$, then the voltage of A is equal to GND.

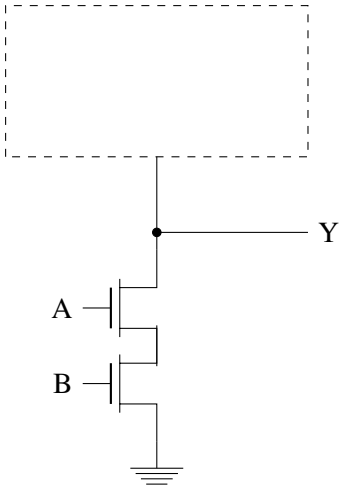
An inverter can be implemented with 1 nMOS and 1 pMOS, as shown in the figure below. When the input A is 0, then the nMOS is OFF and the pMOS is ON. Thus, the output Y is pulled up to 1 because it is connected to V_{DD}. Conversely, when A is 1, then the nMOS is ON and the pMOS is OFF, and Y is pulled down to 0. Therefore, the circuit implements the Boolean formula, $Y = \neg A$.



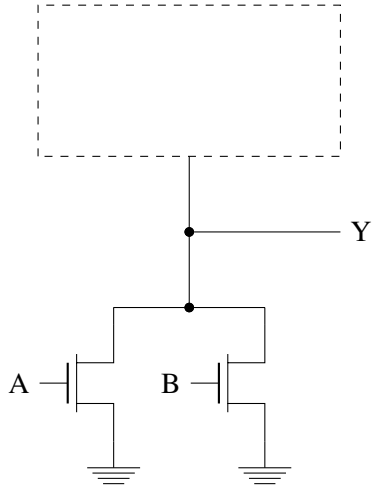
In general, a Boolean-formula circuit has an nMOS *pull-down network* to connect the output to 0 (GND) and a pMOS *pull-up network* to connect the output to 1 (V_{DD}). The pull-up and pull-down networks in the inverter example each consist of a single transistor.

In this problem, we will ask you to design pull-up networks when pull-down networks are given.

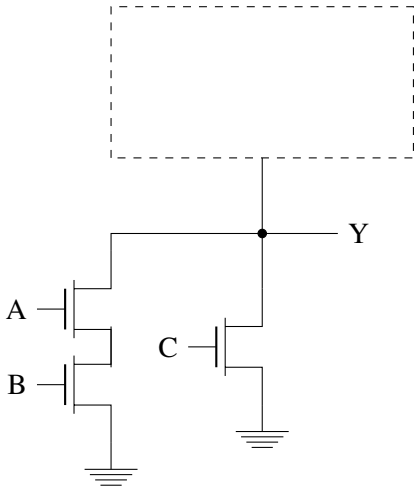
(a) The pull-down network of the Boolean formula (a 2-input NAND gate), $Y = \neg(A \wedge B)$, is given below. Design the pull-up network (the dashed box) with 2 pMOS transistors.



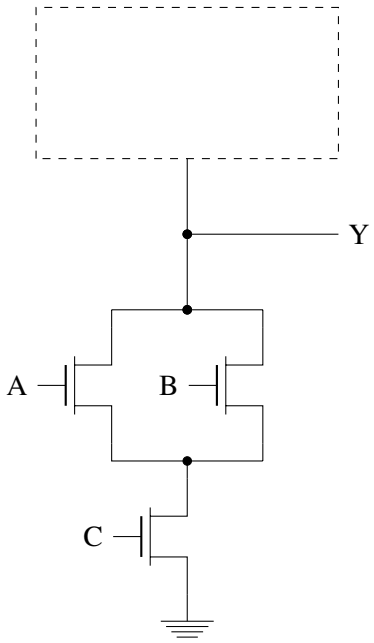
(b) The pull-down network of the Boolean formula (a 2-input NOR gate), $Y = \neg(A \vee B)$, is given below. Design the pull-up network (the dashed box) with 2 pMOS transistors.



(c) The pull-down network of the Boolean formula, $Y = \neg\big((A \wedge B) \vee C\big)$, is given below. Design the pull-up network (the dashed box) with 3 pMOS transistors.



(d) The pull-down network of the Boolean formula, $Y = \neg\big((A \vee B) \wedge C\big)$, is given below. Design the pull-up network (the dashed box) with 3 pMOS transistors.

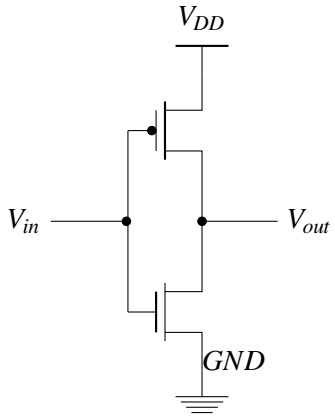


(e) You have designed four pull-up networks. What can you conclude about the rules for designing pull-up networks when pull-down networks are given?

6. From Transistors to Inverter

The following circuit is an inverter built with one pMOS and one nMOS transistor. We assume V_{out} is connected to the input of another identical inverter (not shown). We also assume there is a capacitance connected between V_{out} and GND. In real transistors, this capacitance arises from a combination of capacitances contributed by the transistors of both the inverter in question and any inverters connected to the output. For the moment, we'll just call this capacitance C_L (for load). The resistances associated with the pMOS and nMOS are R_{onP} and R_{onN} , respectively. Let the threshold voltage of the pMOS be V_{tp}, while that for the nMOS be V_{tn}. We will now model the action of the inverter as an RC circuit with two switches controlled by V_{in} as what we did in lectures.

(a) For starters, what are the on-off conditions of the two switches? Please draw the RC circuit modeling this inverter.



(b) Assume $V_{in} = V_{DD}$ for $t < 0$, and $V_{in} = 0$ for $t \geq 0$. In other words, we are assuming the input to our inverter can switch states infinitely fast (this is not true in real life, but gives us a good lower bound on how fast an inverter can switch). How much energy does it take to fully charge C_L?

(c) Given the same condition as in (b), write down the differential equation that describes $V_{out}(t)$ for $t \geq 0$.

(d) What is the solution to this differential equation? Plot $V_{out}(t)$ for $t > 0$.

(e) The term *propagation delay* is used to describe the amount of time it takes between when the input reaches $\frac{V_{DD}}{2}$ and when the output reaches $\frac{V_{DD}}{2}$. Calculate the propagation delay for our inverter above (keep in mind that the input to our inverter changes instantly). Is propagation delay a function of V_{DD}?

(f) Now consider a serial chain of inverters, each driving the one before it. If we assume that $|V_{tn}| = |V_{tp}| = \frac{V_{DD}}{2}$ what is the propagation delay for one of these inverters, given (d) and (e)? (If you like, ignore the first inverter and assume it is driven by an input as in (a)). Here we let $R_{onP} = R_{onN} = R$.

(g) Now let's consider the following scenario: there are N inverters on the chip in your cell phone. It takes **E** Joules of energy to charge all of the inverters at once (from zero to V_{DD}). What is the value of C_L?

(h) Here we interpret a voltage V as logic "1" when $V > \frac{V_{DD}}{2}$, and logic "0" when $V < \frac{V_{DD}}{2}$. Let's assume the maximum frequency, f, at which an inverter can switch back and forth between logic "0" and logic "1" at the output is the inverse of the propagation delay (i.e. we can only switch as fast as one propagation delay). Find an expression that links f, C_L, and R.

Contributors:

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