1   First-Order Differential Equation Practice
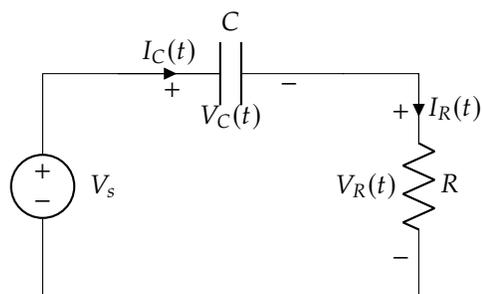
a) Solve the equation $\frac{d}{dt}f(t) = 2f(t)$ given that $f(0) = 5$.

b) Solve the equation $3\frac{d}{dt}f(t) + 6f(t) = 0$ given that $f(0) = 7$.

c) Solve the equation $3f(t) - 6\frac{d}{dt}f(t) = 4$ given that $f(2) = \frac{1}{3}$.

d) Solve the equation $f(t) - a\frac{d}{dt}f(t) = b$, given that $f(t_0) = b$ and $a \neq 0$.

2   RC Circuit

a) Find a differential equation for $V_c(t)$ for $t \geq 0$. Solve the differential equation using the initial condition $V_c(0) = 1\text{V}$. Use component values of $C = 1\text{fF}$ ($1\text{fF} = 10^{-15}\text{F}$), $R = 10\text{k}\Omega$, and $V_s = 2\text{V}$

b) Instead of having an initial condition of $V_c(0) = 1\text{V}$, we now have an initial condition of $I_R(0) = 150\mu\text{A}$ ($1\mu\text{A} = 10^{-6}\text{A}$). Find the new expression for $V_C(t)$ for $t \geq 0$. Use the same component values listed in part (a)

3 Transistor Switch Model

We can improve our resistor-switch model of the transistor by adding in a gate capacitance. In this model, the gate capacitance C_G represents the lumped physical capacitance present on the gate node of all transistor devices. This capacitance is important as it determines the delay of a transistor logic chain.

(a)   NMOS Transistor Resistor-switch-capacitor model

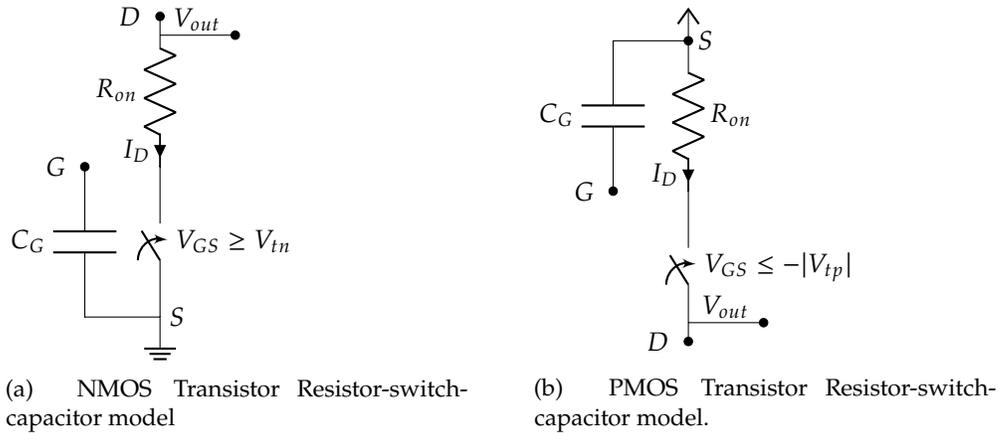(b)   PMOS Transistor Resistor-switch-capacitor model.

Figure 1: Note: We have drawn this so that it aligns with the inverter shown below.

You have two CMOS inverters made from NMOS and PMOS devices. Both NMOS and PMOS devices have an "on resistance" of $R_{on} = 1 \text{ k}\Omega$, and each has a gate capacitance (input capacitance) of $C_G = 1\text{fF}$ (femto-Farads $= 10^{-15}$). The supply voltage V_{DD} is 1Vand the two inverters are connected in series, with the output of the first inverter driving the input of the second inverter (fig. 2).
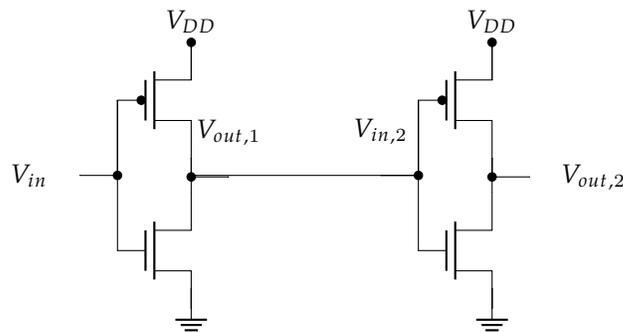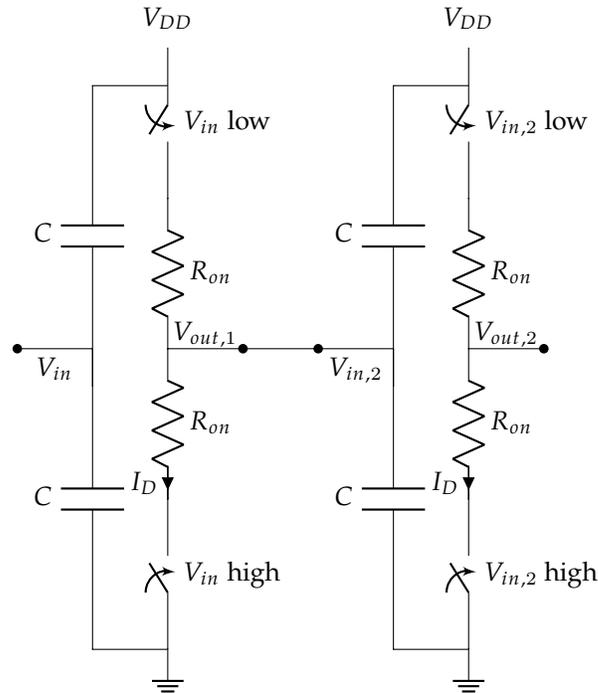

Figure 2: CMOS Inverter chain

Figure 3: Inverter Transistor Resistor-switch model

a) Assume the input to the first inverter has been low ($V_{in} = 0$ V) for a long time, and then switches at time $t = 0$ to high ($V_{in} = V_{DD}$). **Draw a simple RC circuit and write a differential equation describing the output voltage of the first inverter ($V_{out,1}$) for time $t \geq 0$.** Don't forget that the second inverter is "loading" the output of the first inverter — you need to think about both of them.

b) Given the initial conditions in part (a), **solve for $V_{out,1}(t)$.**

c) **Sketch the output voltage of the first inverter, showing clearly (1) the initial value, (2) the initial slope, (3) the asymptotic value, and (4) the time that it takes for the voltage to decay to roughly 1/3 of its initial value.**

d) A long time later, the input to the first inverter switches low again. **Solve for $V_{out,1}(t)$.**

e) **Sketch the output voltage of the first inverter ($V_{out,1}$), showing clearly (1) the initial value, (2) the initial slope, and (3) the asymptotic value.**

f) For each complete input cycle described above ($V_{in} = 0\text{V} \rightarrow 1\text{V} \rightarrow 0\text{V}$), **how much charge is pulled out of the power supply?** Give both a symbolic and numerical answer. **Consider only the charge needed to charge up the $V_{out,1}$ node.**

4   CMOS Scaling

Jerry wants to create a new machine learning accelerator chip using CMOS technology. When designing his chip, he considers the most important parameters of his design to be the amount of energy dissipated when the gate transitions and the delay time it takes for the output of a gate to hit $\frac{V_{DD}}{2}$ from either ground or V_{DD} (i.e. the delay of the gate). These two parameters are very important for CMOS technology, as they determine how quickly the processor can run and how much power it will consume.

Jerry has access to two different fabrication processes: process A and process B.

Process A uses a supply voltage of $V_{DD} = 1\text{V}$. The transistors have a parasitic resistance of $R_p = 10\text{k}\Omega$, and the output driven by a representative inverter has a parasitic capacitance of $C_p = 5\text{fF}$.

Process B uses a supply voltage of $V_{DD} = 3\text{V}$. The transistors have a parasitic resistance of $R_p = 30\text{k}\Omega$, and the output driven by a representative inverter has a parasitic capacitance of $C_p = 1\text{fF}$.

In order to determine which process is better for the design, Jerry decides to analyze the circuit where the input of an inverter transitions from V_{DD} to 0. This can be modeled as the following circuit:
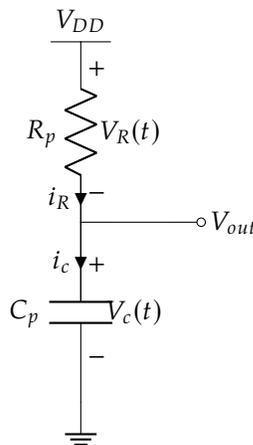
Since the input of the inverter is transitioning from V_{DD} to 0, the initial condition for $V_c(t)$ is:

$$V_c(0) = 0$$

a) In terms of the variables V_{DD}, R_p, and C_p, **solve for** $V_{out}(t)$.

b) Using the expression for $V_{out}(t)$ that was just calculated, **solve for** $i_R(t)$. Keep this expression in terms of the variables V_{DD}, R_p, and C_p.

c) In the previous part, you should have noticed that $i_R(t)$ started at some value, and decayed towards 0 as $t \to \infty$.

   Why does this trend make sense? If the voltage were switching to a different level, would the same trend in current hold?

d) Using the values of V_{DD}, R_p, and C_p from process A, **calculate the time it takes for V_{out} to reach** $\frac{V_{DD}}{2}$.

e) Using the values of V_{DD}, R_p, and C_p from process A, **calculate the total energy delivered by the voltage source, V_{DD}, while the capacitor is being charged to V_{DD}.**

For this problem, recall that the instantaneous power delivered by a voltage source is $P(t) = I(t) \cdot V(t)$. Note that the current and voltage are functions of time.

Energy can be found by integrating power:

$$E = \int_{t=0}^{t=\infty} P(t)dt$$

Remember that the units of energy are Joules [J], while the units of power are Watts [W], which is energy per time: $1\text{W} = \frac{1\text{J}}{1\text{s}}$

f) **Repeat parts (d) and (e), but with the values from process B.**

g) **Compare the energy and delay of process A and B.**

h) Jerry's friend Pat tells Jerry that with process B, one can reduce V_{DD} to 2V. However, the reduction in supply voltage increases the parasitic resistance R_p to $50\text{k}\Omega$. **Calculate the new delay and energy.**

i) Based on your previous answers, **which process should Jerry choose to use? Why?**

5   Homework Process and Study Group

Citing sources and collaborators are an important part of life, including being a student!
We also want to understand what resources you find helpful and how much time homework is taking, so we can change things in the future if possible.

a) **What sources (if any) did you use as you worked through the homework?**

b) **If you worked with someone on this homework, who did you work with?**
   List names and student ID's. (In case of homework party, you can also just describe the group.)

c) **Roughly how many total hours did you work on this homework?**

d) **Do you have any feedback on this homework assignment?**