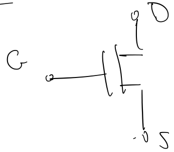
CMOS = complementary metal-oxide semiconductor; Intro to differential eqns

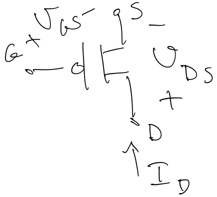
Thursday, September 3, 2020 8:49 AM

Last Time

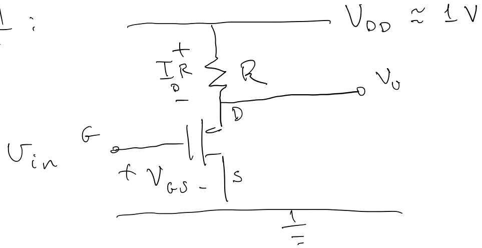
NMOS



PMOS



Ex 1:

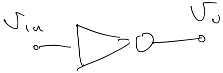


$$v_{in} = 0V \Rightarrow \begin{cases} \text{NMOS device off} \\ \quad \text{(switch OFF)} \\ I_D = 0 \\ v_o = V_{DD} \end{cases}$$

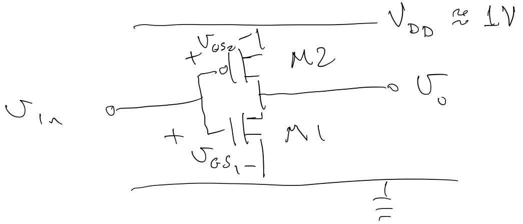
$$v_{in} = V_{DD} \Rightarrow \left\{ \begin{array}{l} v_{GS} > V_{TH} \quad \text{device ON} \\ \text{switch ON} \\ v_{DS} \approx 0 \\ v_o = 0\,\text{V} \\ I_D \neq 0 \end{array} \right.$$

Input		Output	
$v_{in}=0$	Low	$v_o = V_{DD}$	High
$v_{in}=V_{DD}$	High	$v_o = 0$	Low

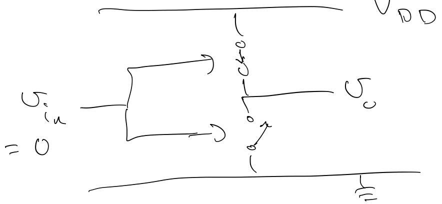
This is an inverter:



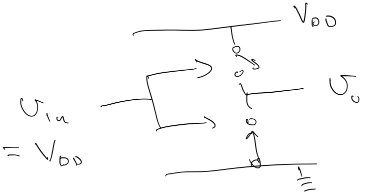
Ex2: Replace R with PMOS



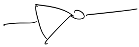
$$1)\ v_{in} = 0 \Rightarrow \left\{ \begin{array}{lll} M1 & \text{OFF} & v_{GS_1} = 0 \\ M2 & \text{ON} & v_{GS_2} = -V_{DD} \end{array} \right.$$



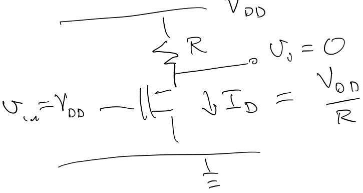
2) $v_{in} = V_{DD} \Rightarrow \begin{cases} M1 \text{ ON } v_{GS_1} = V_{DD} \\ M2 \text{ OFF } v_{GS_2} = 0 \end{cases}$



Logically: This is also an inverter.



For ON state of



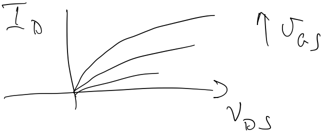
ideal NMOS: $v_{DS} = 0$

power delivered: $\underbrace{V_{DD}}_{} \cdot \underbrace{\frac{V_{DD}}{R}}_{I_D} = \frac{V_{DD}^2}{R}$

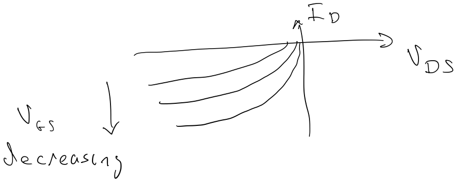
Not wonderful

For CMOS inverter:
- static current ideally zero
- thus an efficient technology

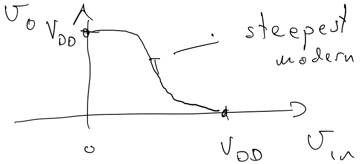
NMOS



PMOS



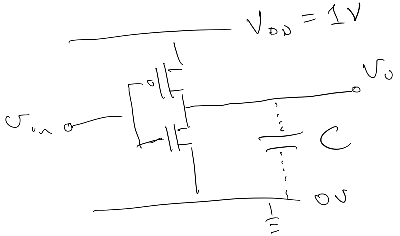
CMOS inverter char.

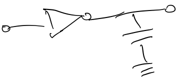


steepest slope with modern tech: ≈ −10

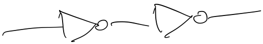
More granular look at power flow in our CMOS inverter

idealized CMOS Inverter



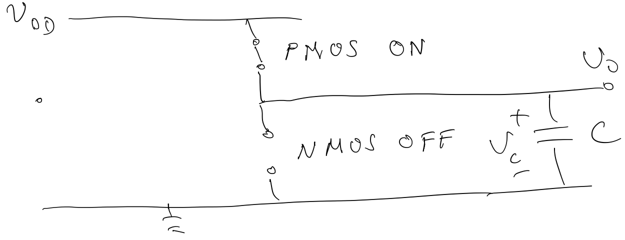


why capacitance C ?

Ex. 

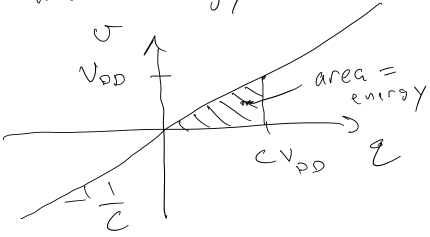
For each NMOS & each PMOS device, have gate capacitance C_{GS}

- maybe will label C_G



$v_c = v_o = V_{DD}$

How much energy stored on cap?



$q = Cv$

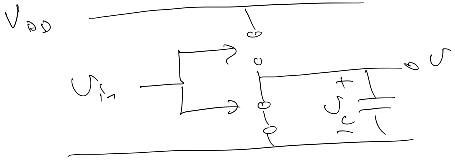
$v = \frac{1}{C} q$

- Energy on cap

$$\int_0^{t_f} v\, i\, dt = \int_0^{t_f} v \frac{dq}{dt}\, dt = \int_0^{CV_{DD}} v\, dq$$

- Energy $= \frac{1}{2} C V_{DD}^2$

- Input of inverter goes from low to high:
  - Output goes low
  - PMOS turns OFF
  - NMOS turns ON ⇒ shorts out capacitor



$E = \frac{1}{2} C V_{DD}^2$ is lost,

expect this energy dissipated in finite resistance of NMOS

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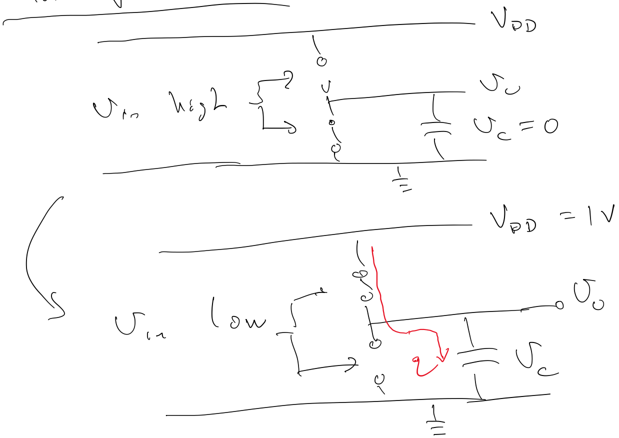
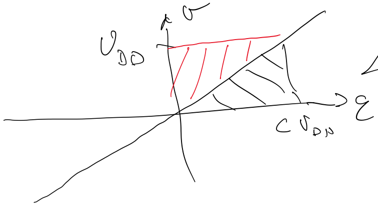
v_{in} goes low





fill up cap again

$\frac{1}{2} C V_{DD}^2$

Any energy dissipated in charging cap?

- class notes: yes, some dissipation occurred, in PMOS

- total charge delivered to cap is

$q_{total} = C V_{DD}$

results in energy $\frac{1}{2} C V_{DD}^2$

but energy delivered from sourle V_{DD}:

$$\underbrace{C V_{DD}}_{\Delta q} \cdot \underbrace{V_{DD}}_{\text{value of dc source}} = C V_{DD}^2$$

– also dissipated $\frac{1}{2} C V_{DD}^2$ when charging cap

Full cycle:

(i) Output high to low:
[Input low to high] lost $\frac{1}{2} C V_{DD}^2$ in NMOS

(ii) Output low to high:
[Input high to low] – replenished cap
– lost $\frac{1}{2} C V_{DD}^2$ in PMOS
– $C V_{DD}^2$ flowed out of V_{DD}

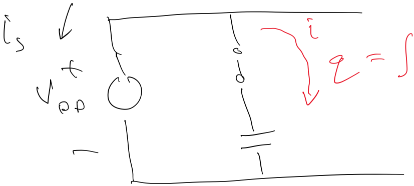
CMOS begins as ideal, but has non-zero power diss:

Dynamic power (i) $CV_{DD}^2 \cdot f_s$: f_s = frequency of clock

Leakage (ii) leakage: "OFF" not really off

Short-ckt (iii) short-circuit current
refers to very small current flow
when maybe PMOS & NMOS
on at same time

Power from source



$q = \int i\, dt$

$$E_s = \int_0^\infty V_{DD}\, i_s\, dt$$

$i = -i_s$

$$= V_{DD} \int_0^\infty (-i)\, dt$$

$$= V_{DD}(-\Delta q) = V_D(-CV_{DD})$$

$$= -CV_{DD}^2$$