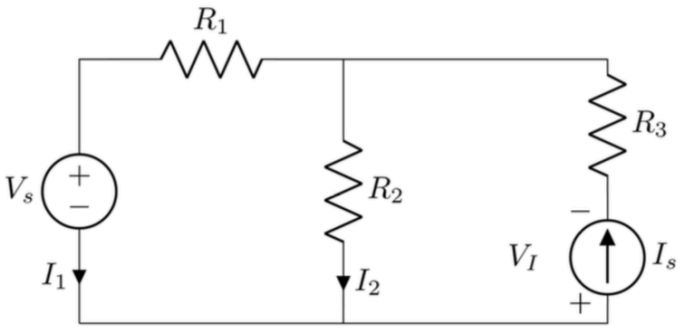
You are given the following circuit:




Which of the following statements are true? [Note: Positive power dissipation indicates that the element is dissipating power while negative power dissipation indicates that the element is generating power.]

1. The power dissipated by all elements must sum to 0.
2. According to Ohm's law, the power dissipated by the resistors must be non-negative.
3. The power dissipated by the voltage source must be less than 0.





4. The power dissipated by the current source $P_I$ may be found by shorting the voltage source, finding $V_I$, and then calculating $P_I = V_I I_S$.

- 1 and 2 only.
- 1, 2, and 3 only.
- 1, 2, 3, and 4.
- 2, 3, and 4 only.
- 1, 3, and 4 only.

# SP2020 FINAL A QUESTION 10

1. "The power dissipated by all elements must sum to 0."

→ Law of Conservation of Energy - energy can neither be created nor destroyed

** if power dissipated > 0, it implies energy was destroyed

*** if power dissipated < 0, it implies energy was created

2. Power dissipated by resistors must be nonnegative.

→ $P = VI = (IR)I = I^2R$

$I^2$ is always positive, R is always positive

∴ P dissipated by resistor is always positive

3. Power dissipated by the voltage source must be less than 0.

→ $P = VI$ ... just need one of $V_s$ or $I$, to be negative in this case

→ It's okay for voltage source to dissi-

pate power... there is a current source to compensate by generating

4. The power dissipated by current source may be found by shorting the voltage source, finding $V_I$, and calculating $P_I = V_I I_s$.

→ Superposition doesn't work like that! Need to also remove current ource and do circuit analysis to find final $V_I$ value.

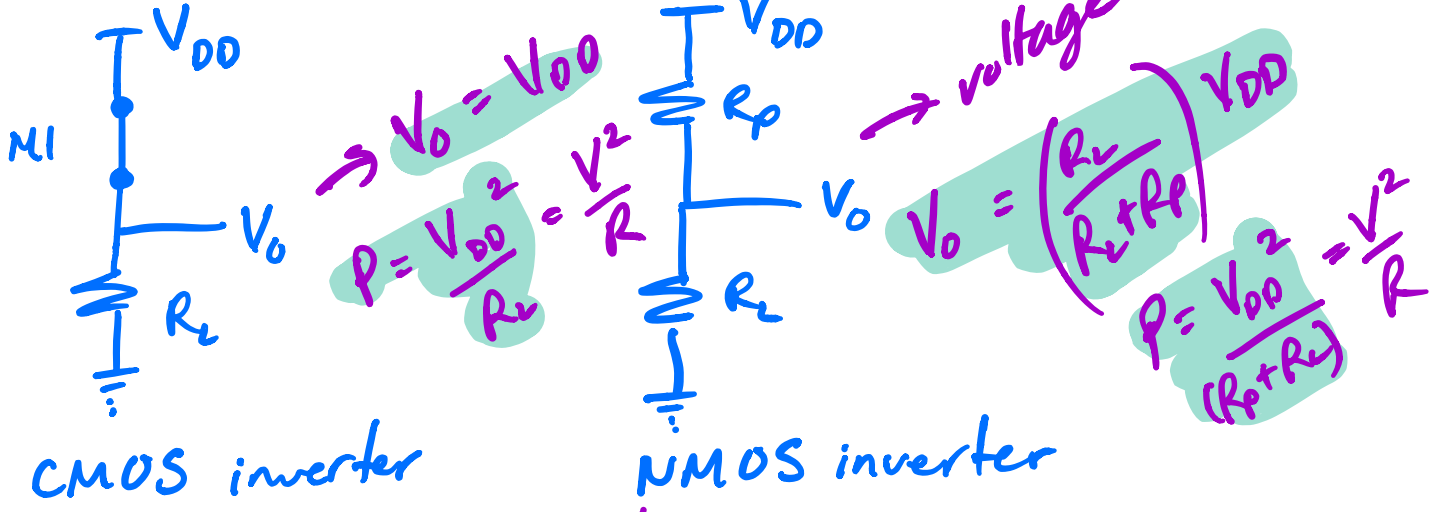
# SP2020 FINAL B QUESTION 8

- goal: advantage of CMOS inverter over NMOS in context of power consumption and output voltage

* assume transistors don't have internal resistance or capacitance

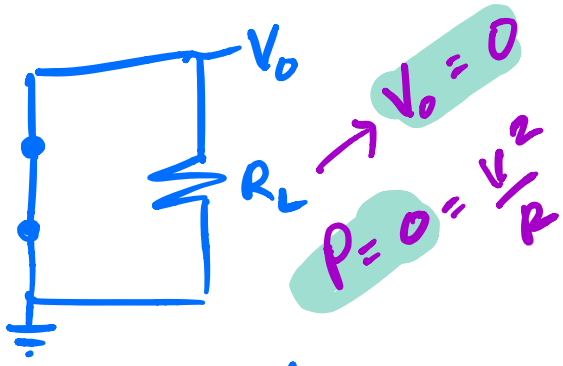
→ draw it out for better intuition

## when M2 is open ($V_{in} \leq V_{th}$)

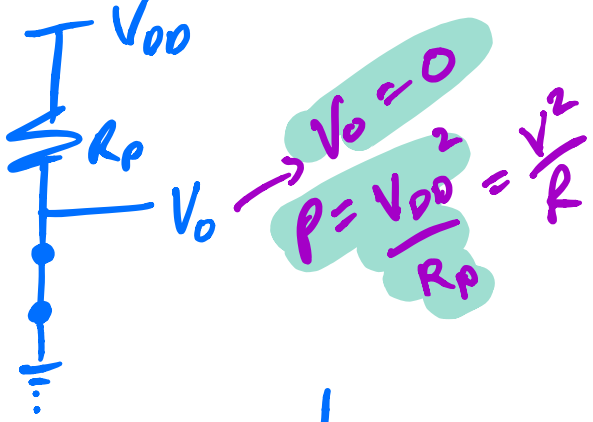



* we can surely conclude the maximum output voltage of CMOS is higher than that of NMOS

## when M2 is closed ($V_{in} > V_{th}$)




CMOS inverter



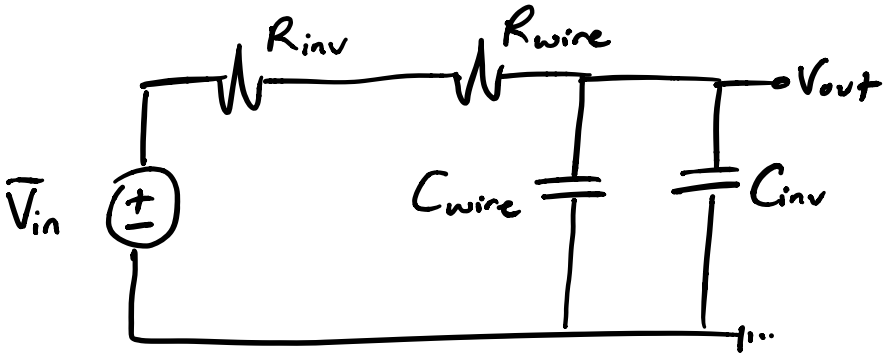

NMOS inverter

* if M2 stays closed (no switching), power consumption of CMOS is lower than that of NMOS

** ILLUSTRATED BOTH CASES PROVING ONLY II AND III

# FA2019 MIDTERM 1 QUESTION 3

(exam on TBP site)

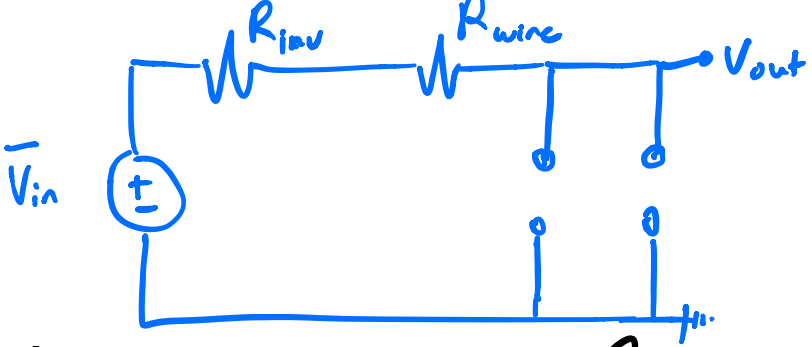



(a) since $\bar{V}_{in} = 0\,V$ for all $t < 0$, at $t = 0$, ckt is in steady state

** mathematically: $\frac{d}{dt} V_{C_{wire}} = 0$; $\frac{d}{dt} V_{C_{inv}} = 0$

$$I_{C_{wire}}(t) = C_{wire} \frac{d}{dt} V_{C_{wire}}(t) = 0 \;@\; t = 0$$

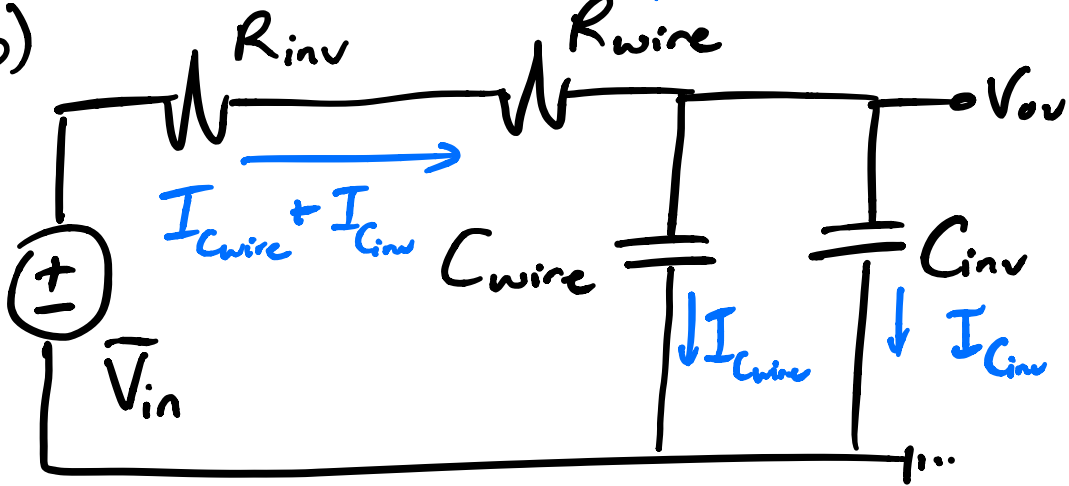
$$I_{C_{inv}}(t) = C_{inv} \frac{d}{dt} V_{C_{inv}}(t) = 0 \;@\; t = 0$$




→ no current

$\therefore V_{out} = \bar{V}_{in} = 0$ @ $t = 0$

(b)



$$Q = CV \; ; \; \frac{d}{dt} Q(t) = C \frac{d}{dt} V(t) = I$$

$$I_{C_{wire}} = C_{wire} \frac{d}{dt} V_{C_{wire}}(t) = C_{wire} \frac{d}{dt} V_{out}(t)$$

$$I_{C_{inv}} = C_{inv} \frac{d}{dt} V_{C_{inv}}(t) = C_{inv} \frac{d}{dt} V_{out}(t)$$

$$V_{out}(t) = \bar{V}_{in}(t) - (R_{inv} + R_{wire})(I_{C_{wire}} + I_{C_{inv}})$$

$$= \bar{V}_{in}(t) - (R_{inv} + R_{wire}) \left( \frac{d}{dt} V_{out}(t) \right) (C_{wire} + C_{inv})$$

$$\frac{d}{dt} V_{out}(t) = \frac{\bar{V}_{in}(t) - V_{out}(t)}{(R_{inv} + R_{wire})(C_{wire} + C_{inv})}$$

(c) $$\tilde{V}(t) = \bar{V}_{in}(t) - V_{out}(t) \; ; \; \frac{d}{dt} \tilde{V}(t) = -\frac{d}{dt} V_{out}(t)$$

$$\frac{d}{dt} \tilde{V}(t) = \frac{-\tilde{V}(t)}{(R_{inv} + R_{wire})(C_{wire} + C_{inv})}$$

$$\lambda = (R_{inv} + R_{wire})(C_{wire} + C_{inv}) \; ; \; \tau = \frac{1}{\lambda}$$

$\lambda = 10^{-7}$, $\tau = 10^{7}$

$$\frac{d}{dt} \tilde{V}(t) = -\tau \tilde{V}(t) \rightarrow \tilde{V}(t) = A e^{-\tau t}$$

$$\frac{d}{dt} \tilde{V}(t) = -\tau (A e^{-\tau t}) = -\tau \tilde{V}(t)$$

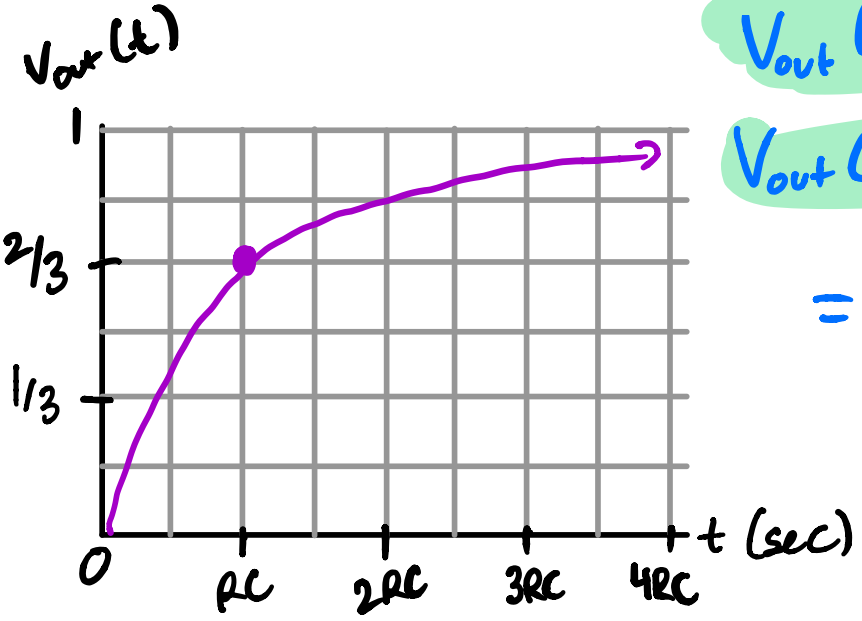
$$\tilde{V}(0) = A e^{-\tau(0)} = A = \bar{V}_{in}(0) - V_{out}(0) = 1\,V$$

($\bar{V}_{in}(0)$: Given; $V_{out}(0)$: part a)

$\tilde{V}(t) = e^{-10^7 t} \rightarrow \bar{V}_{in}(t) - V_{out}(t) = e^{-10^7 t}$

$V_{out}(t) = 1 - e^{-10^7 t}$

(d)



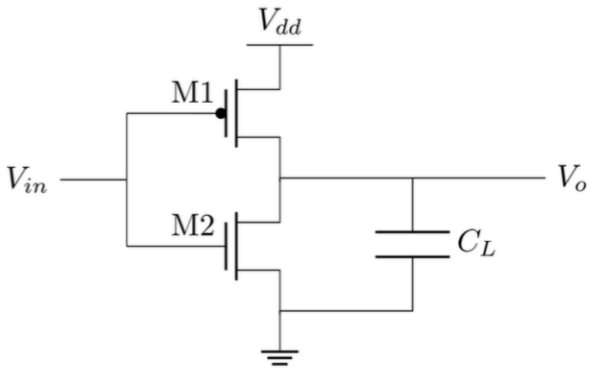

$V_{out}(t)\big|_{t \to \infty} = 1 - e^{-\infty} = 1$ (0)

$V_{out}(t)\big|_{t = RC} = 1 - e^{-10^7 (10^{-7})}$

$= 1 - e^{-10^0} = 1 - e^{-1}$

You are given the inverter circuit shown below. You would like to reduce the power supplied by the power supply by a factor of 2.

You are given that $C_L = 1\ \mathbf{pF}$, $f_s = 1\ \mathbf{GHz}$ (the clock rate), $R_{on,p} = R_{on,n} = 10\Omega$, and $V_{dd} = 1\ \mathbf{V}$. You are only allowed to adjust the circuit as described below. Which of the following could you do?




- Add another PMOS transistor in series with M1 and another NMOS transistor in series with M2.





- None of the other choices.
- Double $C_L$.
- Double $V_{dd}$.
- Add another PMOS transistor in parallel with M1 and another NMOS transistor in parallel with M2.

# Sp2020 Final B Question 9

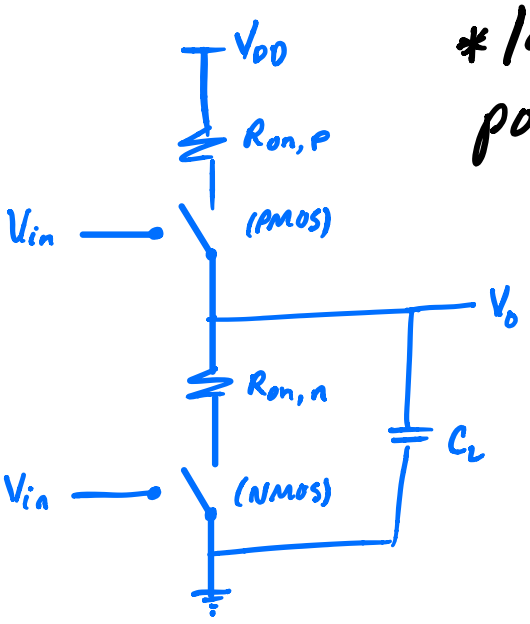
- goal: reduce power supplied by a factor of 2 → $P = VI$

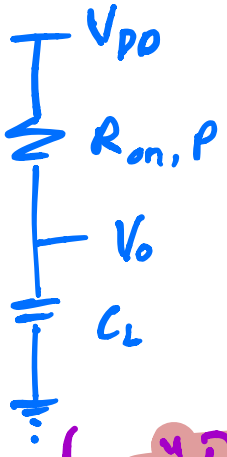
→ so either reduce voltage or current

* we can surely eliminate "Double $V_{DD}$"

→ draw it out for better intuition

* look at circuit from POV that power is being supplied




$$I = C_L \frac{d}{dt} V_o(t)$$

$$= V_{DD} - V_o / R_{on,p}$$

$$P = VI =$$

$$V_{DD} C_L \frac{d}{dt} V_o(t)$$

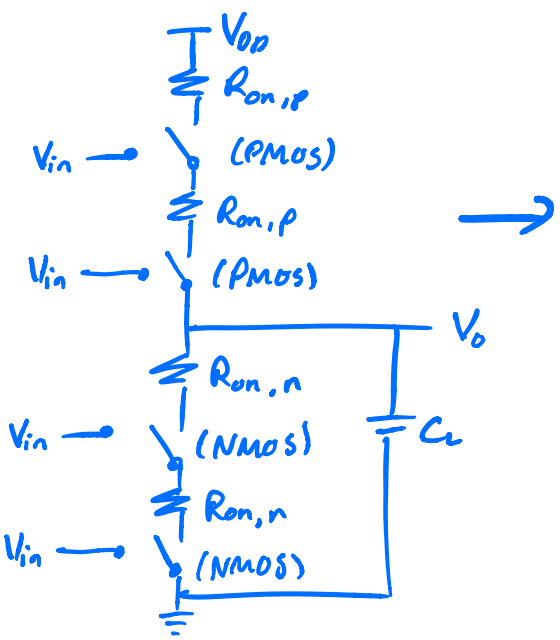
* we can surely eliminate "Double $C_L$"

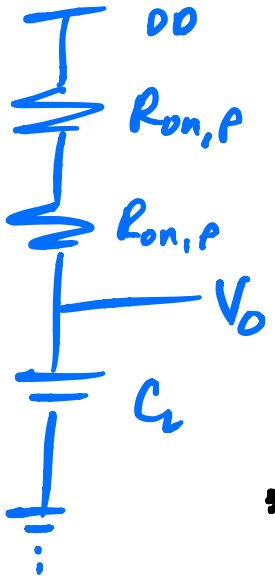
pattern for voltage of a charging capacitor when input voltage is 1V in an RC circuit (based on Fall 2019 MT1):

$$V_c(t) = 1 - e^{-t/RC}$$

$$P = V_{DD} I = \frac{V_{DD}(V_{DD} - V_c)}{R_{on,p}} =$$

$$= \frac{V_{DD}(1 - 1 + e^{-t/RC})}{R_{on,p}} = \frac{V_{DD} e^{-t/R_{on,p} C}}{R_{on,p}}$$



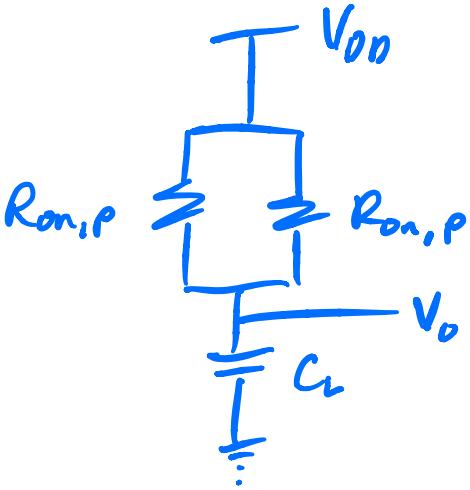

effective R is 2 $R_{on,p}$

$$\rho = \frac{V_{DD}\, e^{-t/2R_{on,p}C}}{2R_{on,p}}$$

* not perfect factor of 2 due to exponent

* we can surely eliminate "Add another PMOS transistor in series..."

(can draw out if you want but you can also realize by inspection)




effective R is 0.5 $R_{on,p}$

$$\rho = \frac{V_{DD}\, e^{-t/0.5R_{on,p}C}}{0.5R_{on,p}}$$

* not even reduced

* we can surely eliminate "Add another PMOS transistor in parallel..."

** LEAVING "None of the other choices"

# SP2020 MIDTERM 1 QUESTION 3 (exam on TBP site)

$e^{j\theta} = j\sin\theta + \cos\theta$ → Euler's Formula

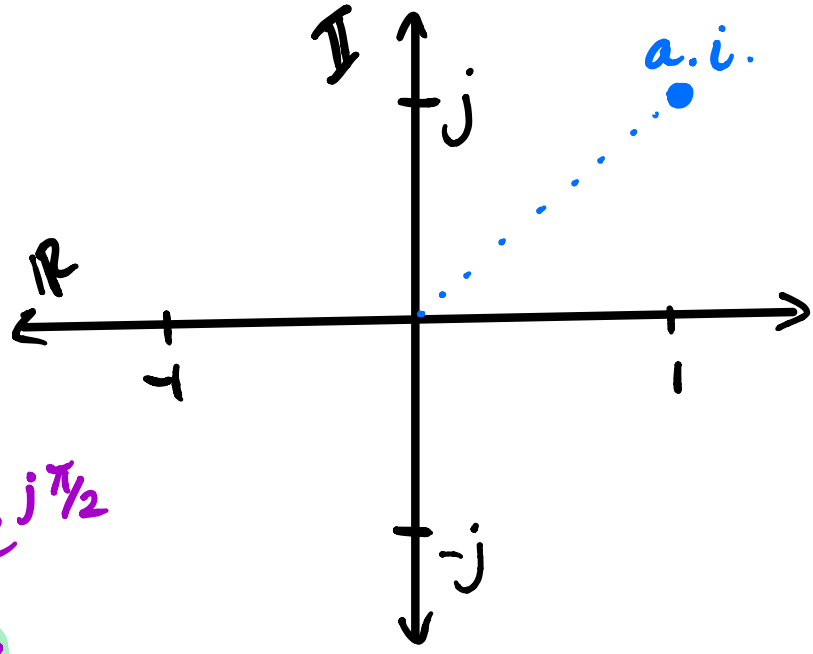
a) i. magnitude = $\sqrt{2}$

↳ $\sqrt{1^2+1^2} = |1+j|$

angle = $45° = \pi/4$

↳ $\arctan(1/1)$

$1+j = \sqrt{2}e^{j\pi/4}$




ii. $\sqrt{j} = j^{1/2}$ $j = e^{j\pi/2}$

$\sqrt{j} = (e^{j\pi/2})^{1/2} = e^{j\pi/4}$

b) i. $3e^{j\pi/3}$ $3e^{j\pi/2} = 3(j\sin\frac{\pi}{3} + \cos\frac{\pi}{3}) =$

$3(j\frac{\sqrt{3}}{2} + \frac{1}{2}) = \frac{3\sqrt{3}}{2}j + \frac{3}{2}$

ii. $-\sqrt{7}e^{\pi j}$ $-\sqrt{7}e^{\pi j} = -\sqrt{7}(j\sin\pi + \cos\pi) =$

method 1: $-\sqrt{7}(j(0) + (-1)) = \sqrt{7}$

method 2: $e^{\pi j} = -1$ $(-\sqrt{7})(-1) = \sqrt{7}$

c) i. $\frac{1}{j} = -j$ ① $\frac{1}{j} \times j = -j \times j$

② $\frac{j}{j} = -(j^2)$ ③ $1 = -(-1)$

④ $1 = 1$ ✓ Q.E.D.

ii. $\sin(2x) = 2\cos x \sin x$

① $e^{j\theta} = j\sin\theta + \cos\theta$

② $e^{-j\theta} = j\sin(-\theta) + \cos(-\theta) = -j\sin\theta + \cos\theta$

positive trig mapping

| Sin | All |
|---|---|
| Tan | Cos |

③a $e^{j\theta} + e^{-j\theta} = j\sin\theta + \cos\theta + (-j\sin\theta + \cos\theta) = 2\cos\theta$

④a $\cos\theta = \dfrac{e^{j\theta} + e^{-j\theta}}{2}$

③b $e^{j\theta} - e^{-j\theta} = j\sin\theta + \cos\theta - (-j\sin\theta + \cos\theta) = 2j\sin\theta$

④b $\sin\theta = \dfrac{e^{j\theta} - e^{-j\theta}}{2j}$

① $\sin(2x) = \dfrac{e^{j(2x)} - e^{-j(2x)}}{2j}$ ✓

② $\cos x \sin x = 2\left(\dfrac{e^{jx} + e^{-jx}}{2}\right)\left(\dfrac{e^{jx} - e^{-jx}}{2j}\right) =$

$\dfrac{(e^{jx})^2 - (e^{-jx})^2}{2j} = \dfrac{e^{j2x} - e^{-j2x}}{2j}$

Q.E.D.