Designing Information Devices and Systems II EECS 16B Discussion 6A Anant Sahai and Michel Maharbiz Spring 2016

1. Two Capacitors

Consider the circuit below, assume that when $t \le 0$, both capacitors have no charge ($V_1(t = 0) = 0$ and $V_2(t=0)=0$). At t=0, the switch closes.



Figure 1: Two Capacitor Circuit with Voltage Source

- (a) First, use Kirchoff's Laws and the capacitor equation $(I = \frac{dV}{dt}C)$ to find the differential equation of this circuit.
- (b) As shown in class, we can write each voltage V(t) as $V_{std}(t) + V_{trans}(t)$, where $V_{std}(t)$ is the steady state function and $V_{trans}(t)$ is the transient function.

What are the steady state functions of $V_1(t)$ and $V_2(t)$?

- (c) Now, replace $V_1(t) = V_{1,std}(t) + V_{1,trans}(t)$ and $V_2(t) = V_{2,std}(t) + V_{2,trans}(t)$ using the steady state functions you found in the previous part. Also, find the initial conditions of $V_{1,trans}(t)$ and $V_{2,trans}(t)$ when t = 0.
- (d) Assume that $C_1 = C_2 = 1$, $R_1 = \frac{1}{3}$, and $R_2 = \frac{1}{2}$. Diagonalize the matrix A in $\frac{d}{dt} \begin{pmatrix} V_{1,trans}(t) \\ V_{2,trans}(t) \end{pmatrix} = \begin{bmatrix} V_{1,trans}(t) \\ V_{2,trans}(t) \end{bmatrix}$ $\begin{bmatrix} V_{1,trans}(t) \\ V_{2,trans}(t) \end{bmatrix}$

$$A \begin{bmatrix} V_{1,trans}(t) \\ V_{2,trans}(t) \end{bmatrix}$$

- (e) Now that we have diagonalized the matrix, we can now work in the eigenspace. Let us call the transformed $\begin{bmatrix} V_{1,trans}(t) \\ V_{2,trans}(t) \end{bmatrix}$ as $\tilde{V}(t) = \begin{bmatrix} \tilde{V}_1(t) \\ \tilde{V}_2(t) \end{bmatrix}$. Solve for $\tilde{V}(t)$. Do not forget about the initial conditions of $\tilde{V}(t)$.
- (f) Now that we have $\tilde{V}(t)$, find the solution for $\begin{vmatrix} V_{1,trans}(t) \\ V_{2,trans}(t) \end{vmatrix}$.
- (g) For the final step, solve for $\begin{bmatrix} V_1(t) \\ V_2(t) \end{bmatrix}$.
- (h) Sketch the voltage vs time plots of $V_1(t)$ and $V_2(t)$.

2. RC Circuit - NAND Let us consider the RC Circuits of a NAND logic gate. This circuit implements the boolean function $\neg(A \land B)$.

As shown in the figure, we can replace all the transistors with a resistor and switch but there is also a capacitor between the nMOS gates in the PUN. This capacitor complicates how long it takes for V_{out} to obtain the correct value. We will see how shortly.

Assume that A and B can only have two voltage values; V_{DD} (1) and Ground (0). A and B can change instantaneously.

- (a) Assume for t < 0, A = 1 and B = 0 for a long enough time. What are the voltages across the two capacitors?
- (b) At t = 0, the inputs change: A = 1 and B = 1. What is the resulting circuit of the NAND? Find the differential equation for V_{out} .
- (c) Assume that $R_1 = \frac{1}{3}$, $R_2 = 1$, $C = \frac{1}{2}$, and $C_L = \frac{1}{3}$. Solve the differential equation in part (b).
- (d) Let us try another situation. Assume for t < 0, A = 0 and B = 1. At t = 0, the inputs change: A = 1 and B = 1. What is the resulting circuit of the NAND? What are the initial conditions for the voltages across the two capacitors? Find the differential equation for V_{out} .
- (e) Assume that $R_1 = \frac{1}{3}$, $R_2 = 1$, $C = \frac{1}{2}$, and $C_L = \frac{1}{3}$. Solve the differential equation in part (d).

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